

Hummingbird1_HR

DIS/UMA/Muxless Schematics Document

Sandy Bridge

Intel PCH

DY :None Installed
DIS:DIS installed
DIS_Muxless :BOTH DIS or Muxless installed
DIS_PX:BOTH DIS or PX installed
DIS_PX_Muxless:DIS or PX or Muxless installed.
Muxless: Muxless installed.(PX4.0)
PX:MUX installed.(PX3.0)
PX_Muxless:BOTH PX or Muxless installed.
UMA:UMA installed
UMA_Muxless:BOTH UMA or Muxless installed
UMA_PX_Muxless:UMA or PX or Muxless installed

ANNIE: ONLY FOR ANNIE solution.
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.

Project code : 91.4QP01.001

PCB P/N :

Revision :

Hummingbird1_HR Block Diagram

SYSTEM DC/DC		CPU DC/DC	
APL5916KAI 48		NCP6131S52MNR 42~43	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
1D05V_PWR	0D85V_S0	DCBATOUT	VCC_CORE

SYSTEM DC/DC	
UP6128PQDD 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC	
UP6183PQAG 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC	
UP6165BQKF 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

SYSTEM DC/DC	
NCP5911MNTBG 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE_PWR

VGA	
RT8208BGQW 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

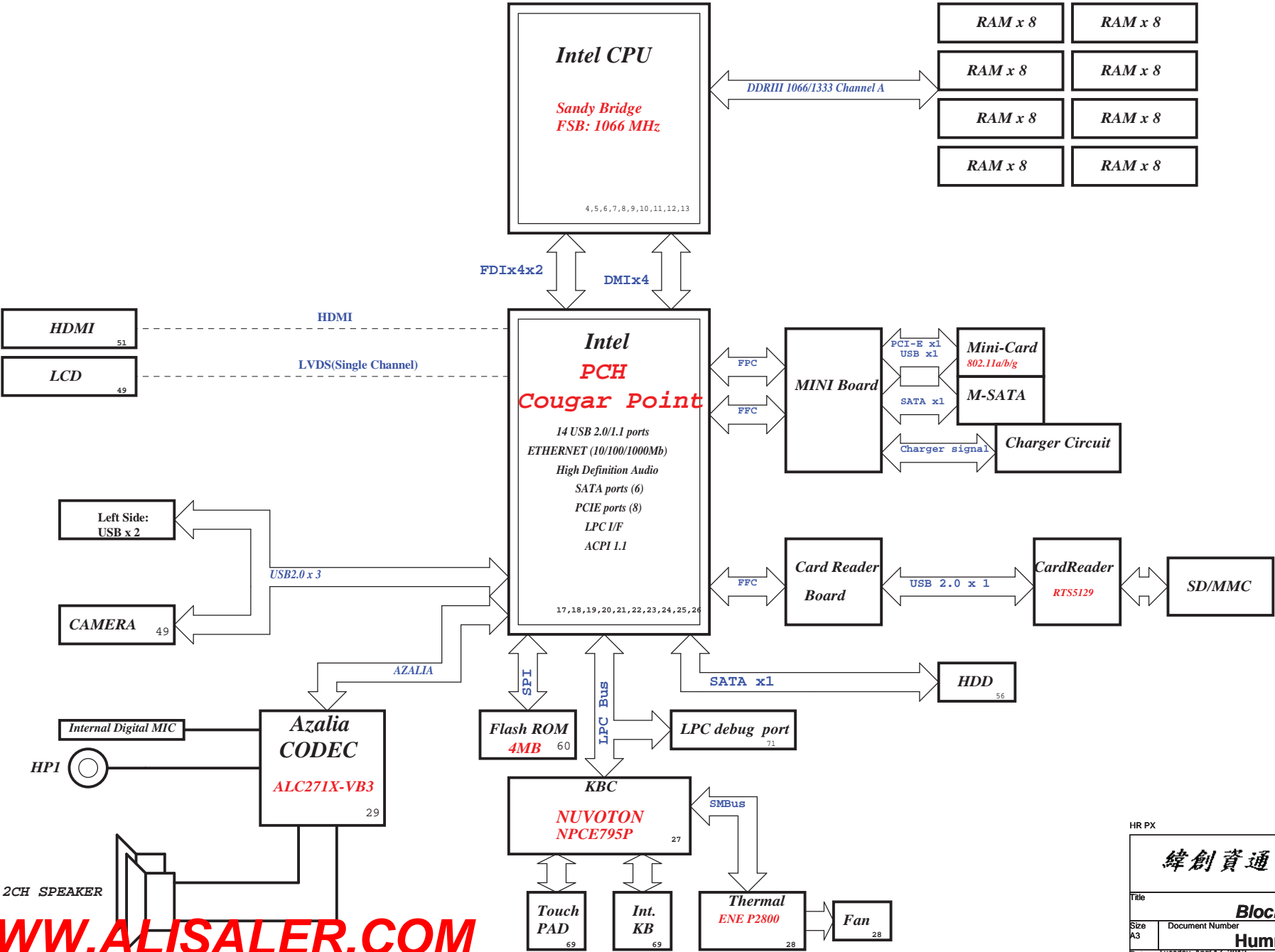
TI CHARGER	
BQ24745RHDR 40	
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC	
RT9025 47	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0

SYSTEM DC/DC	
RT9025-25PSP 93	
INPUTS	OUTPUTS
1D5V_S3 3D3V_S5	1V_VGA_S0 1D8V_VGA_S0

Switches	
INPUTS	OUTPUTS
1D5V_S3 3D3V_S0	1D5V_VGA_S0 3D3V_VGA_S0

PCB LAYER	
L1:Top	L4:Signal
L2:VCC	L5:GND
L3:Signal	L6:Bottom



HR PX

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Title

Block Diagram

Hummingbird1_HR

Size A3

Document Number

Rev -2

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PCB Strapping Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	Enable Danbury: Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. Disable Danbury: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] Disable Danbury: Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

USB Table

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Mini Card1(WLAN)
LANE3	Card Reader
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	OD
5	E-SATA

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA / USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

Processor Strapping Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		Disabled - No Physical Display Port attached to Embedded DisplayPort. 1: Enabled - An external Display Port device is connect to the EMBEDDED display Port	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	PEG DEFER TRAINING	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	

POWER PLANE	VOLTAGE	Voltage Rails	
		ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_OPAKCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

SMBus ADDRESSES

I ² C / SMBus Addresses		Ref Des	HURON RIVER ORB		
Device			Address	Hex	Bus
EC SMBus 1 Battery CHARGER					BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP					SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI					PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

<Variant Name>

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File			
Table of Content			
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Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

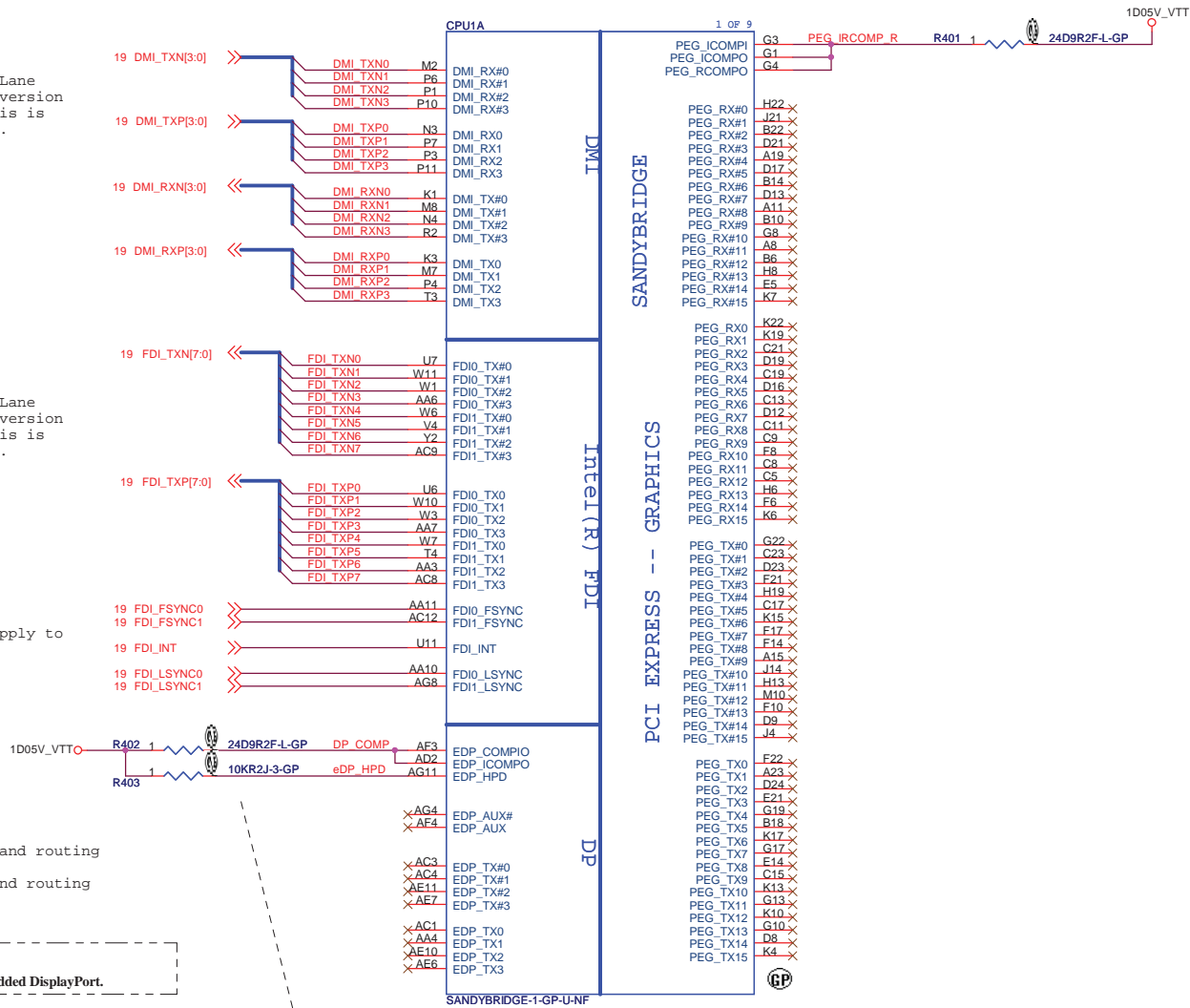
Note:
Lane reversal does not apply to FDI sideband signals.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

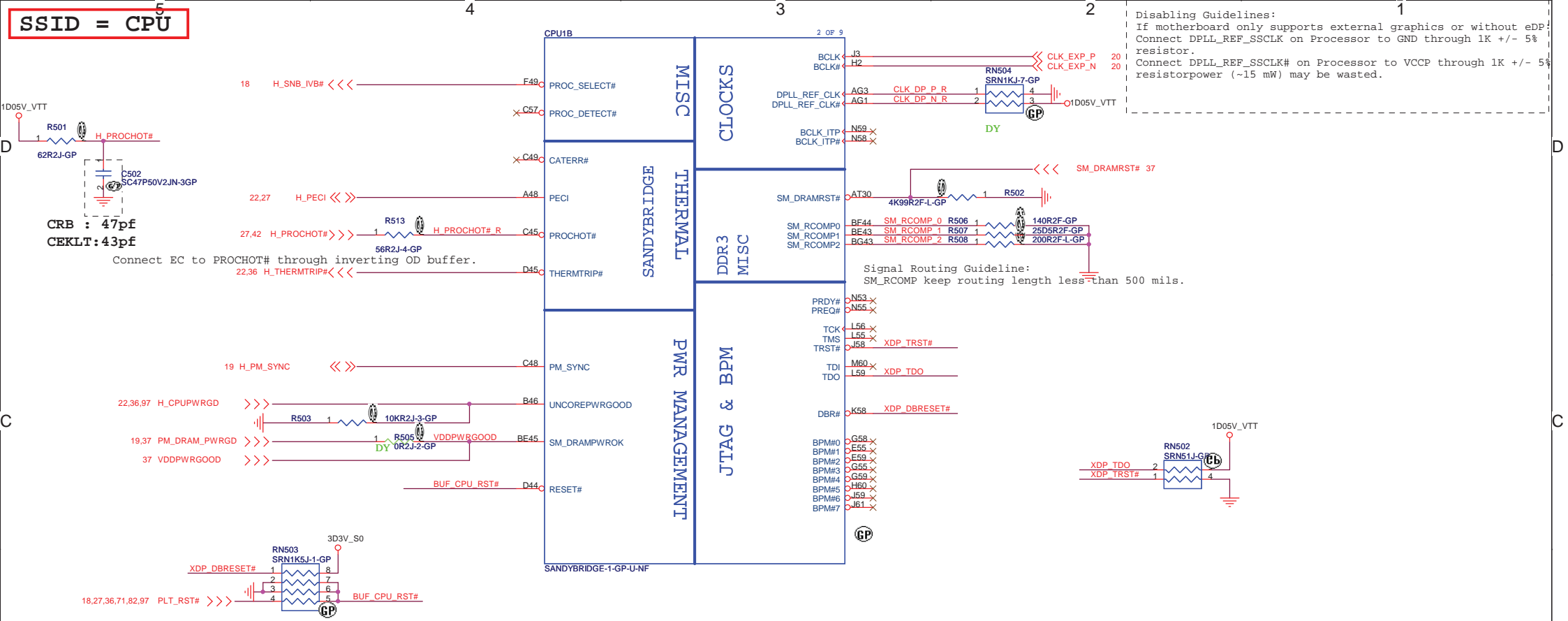
NOTE:
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

NOTE:
Select a Fast FET similar to 2N7002E whose rise/fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

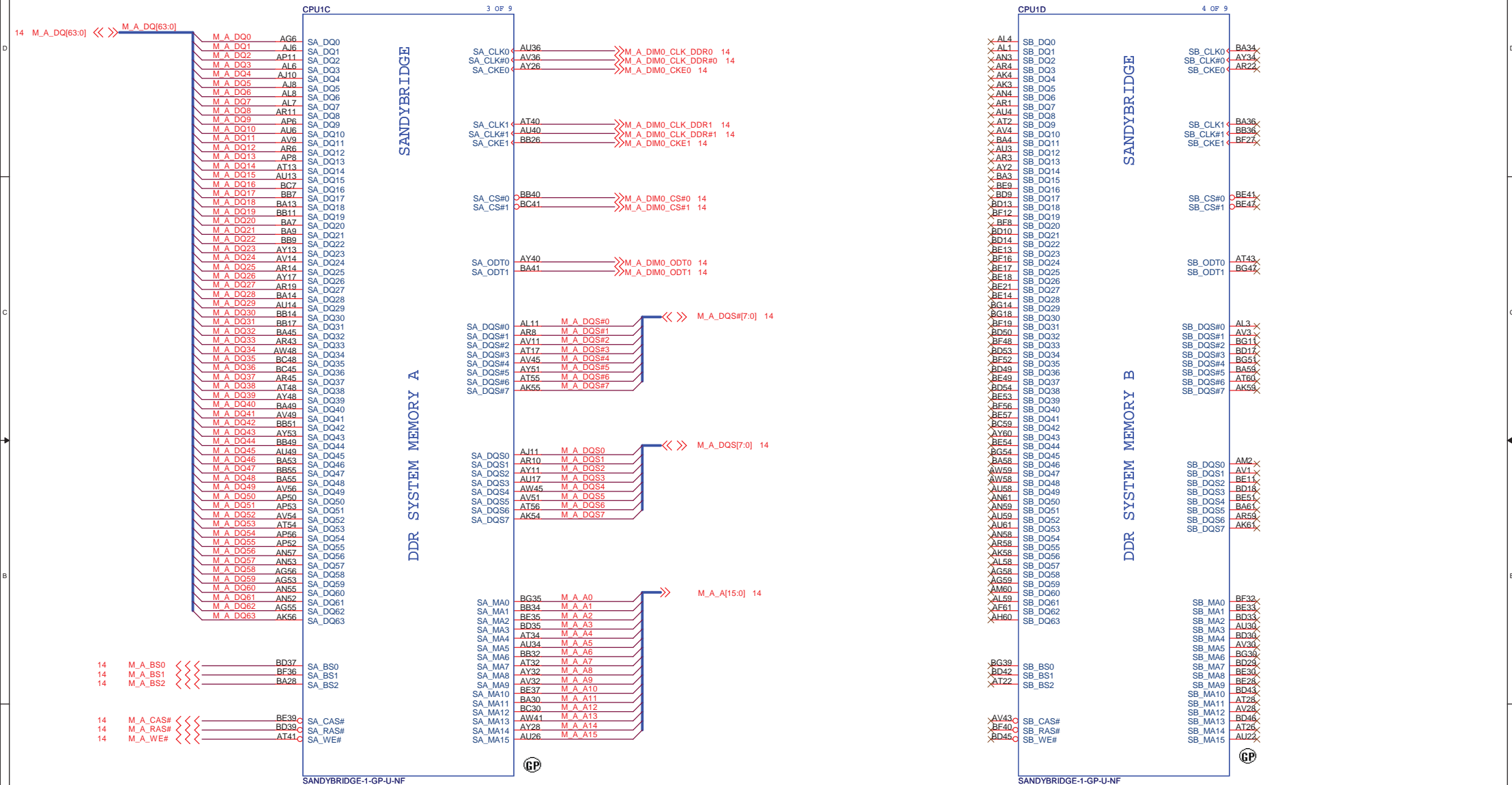


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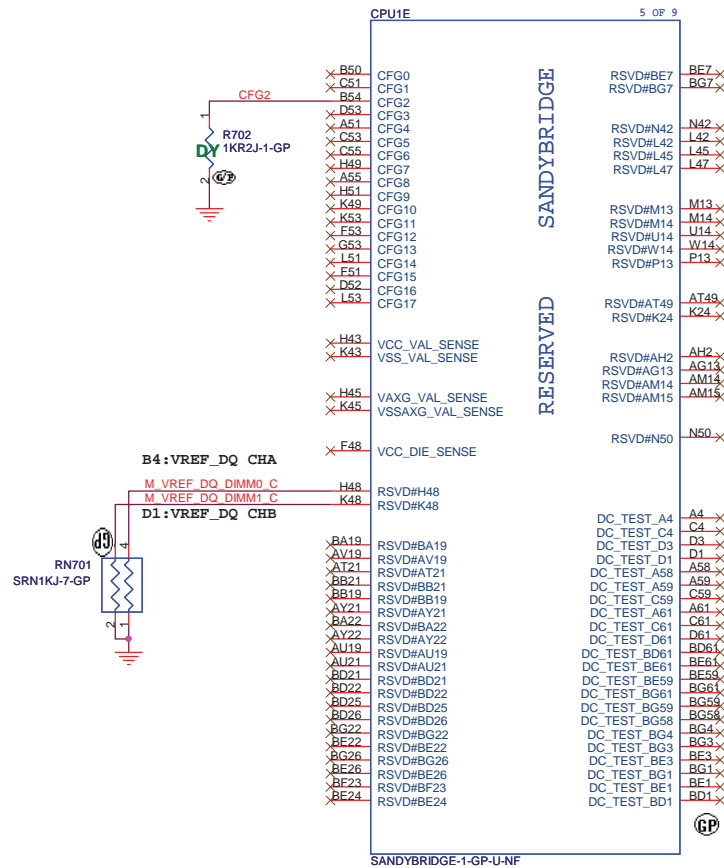


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SSID = CPU



SSID = CPU



PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed

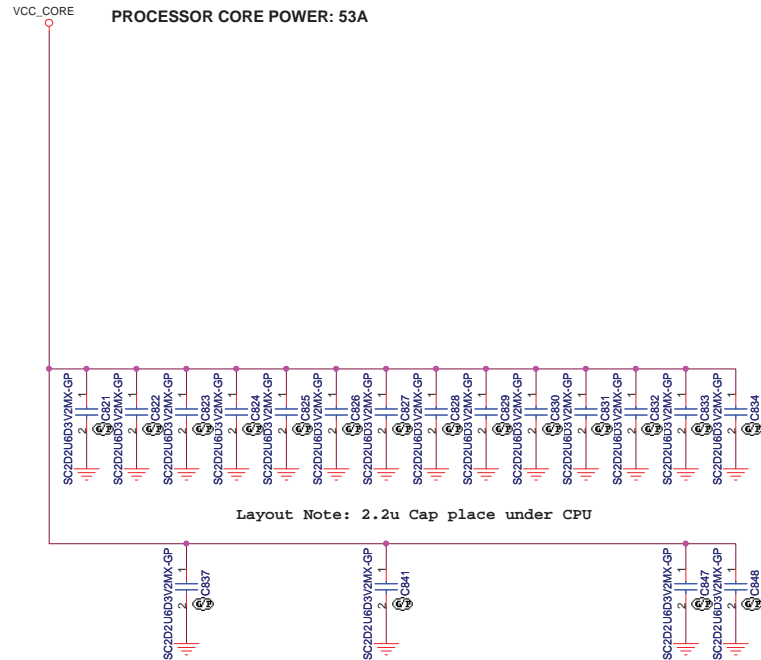
Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

PCIe Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

PEG DEPER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

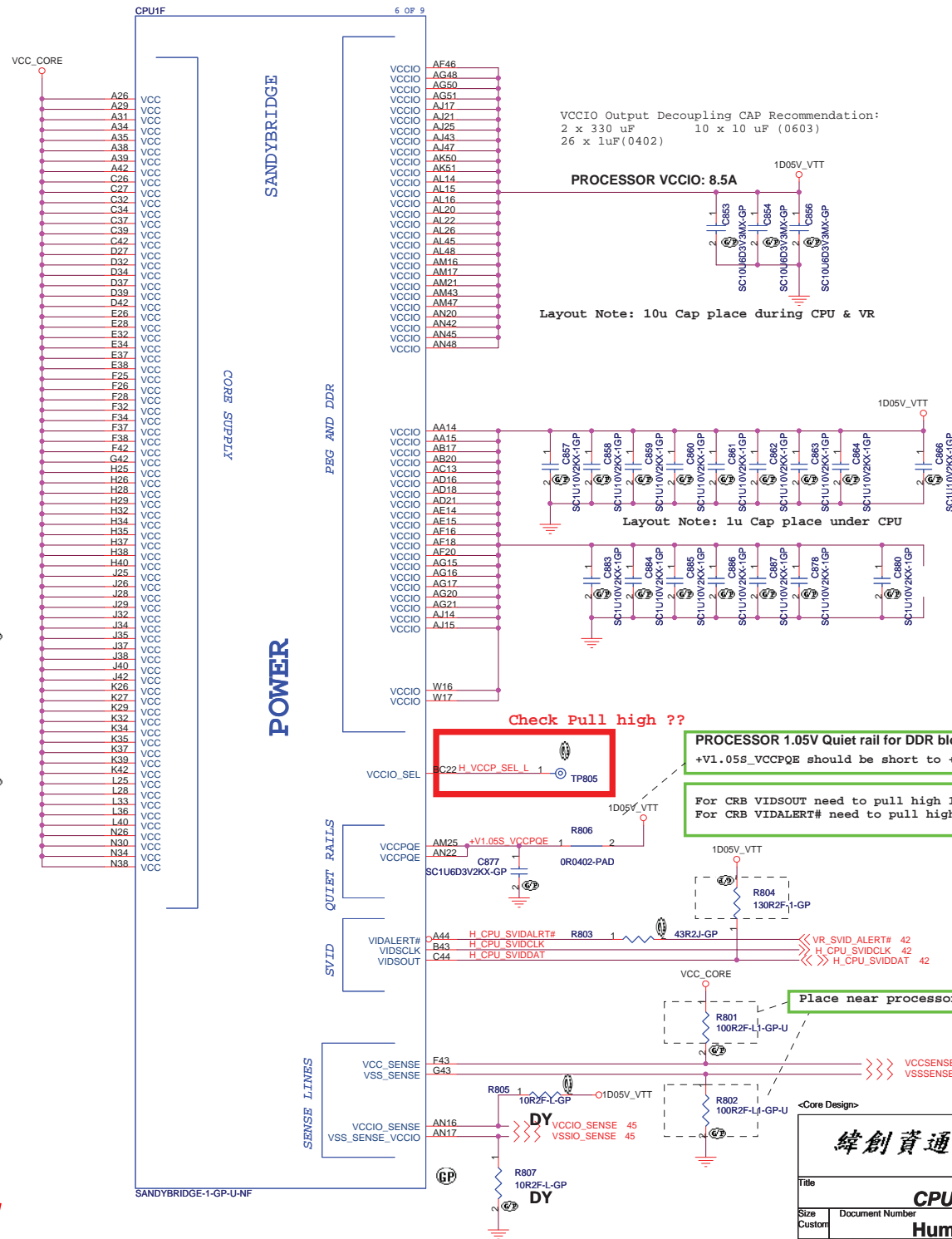
SSID = CPU

Voltage Rail	Voltage	Iccmax
VCC_CORE(QC)	0.8~1.35	94A
VCC_CORE(DC)	0.8~1.35	53A
VCCIO	1.05	8.5A
VDDQ	1.5	10A
VCCSA	0.75~0.9	6A
VCCPLL	1.8	1.2A
VAXG	0~1.52	33A

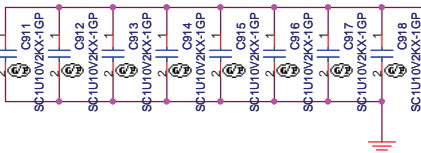


VCC Output Decoupling CAP Recommendation:

1. 1.9m ohm loadline design: (for SW)
 - 4 x 470 uF
 - 25 x 22 uF
 - 35 x 2.2uF
2. 2.9m ohm loadline design: (for ULV/LV)
 - 3 x 330uF
 - 12 x 22uF
 - 16 x 2.2uF

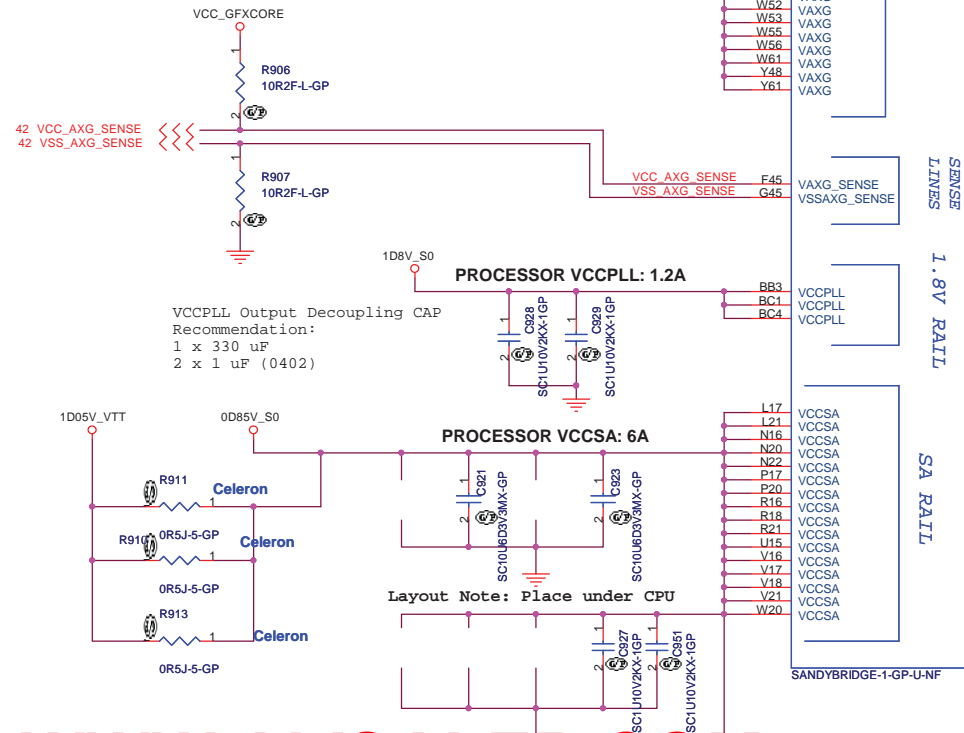


SSID = CPU



```
1. 3.9m ohm loadline design:(for GT2)
2 x 470 uF      6 x 22 uF (0805)
6 x 10 uF (0603) 11 x 1 uF (0402)

2. 4.6m ohm loadline design:(for G1)
2 x 330 uF      5 x 22 uF (0805)
6 x 10 uF (0603) 6 x 1 uF (0402)
```



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CPU1G

SANDYBRIDGE

POWER

GRAPHICS

SENSE
LINES

1.8V RAIL

SA RAIL

SANDYBRIDGE-1-GP-U-NF

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DDR3 - 1.5V RAILS

QUIET RAILS

SENSE LINES

VID0 VCCSA_VI
VID1

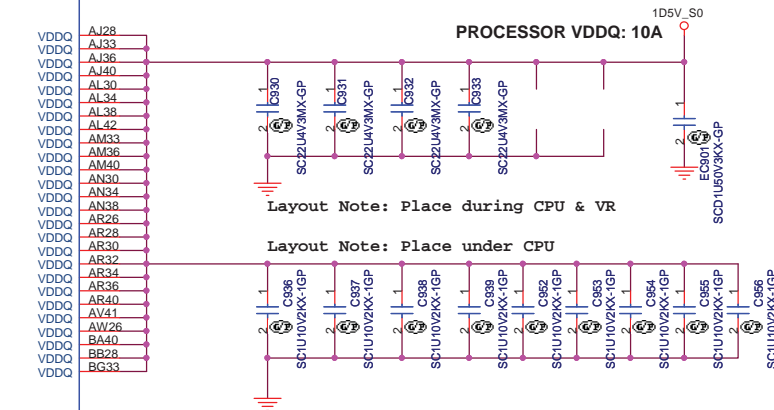
Power Delivery DG; #139028

A 1-K pull-down resistor should be placed on the VCCSA_VID lines.

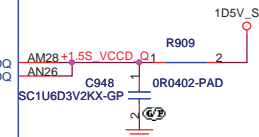
S3 power reduction DDR Vref schematic

Refer to the latest Huron River Mainstream PDG
(Doc# 438297) for more details

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT
should have 10 mils trace width.

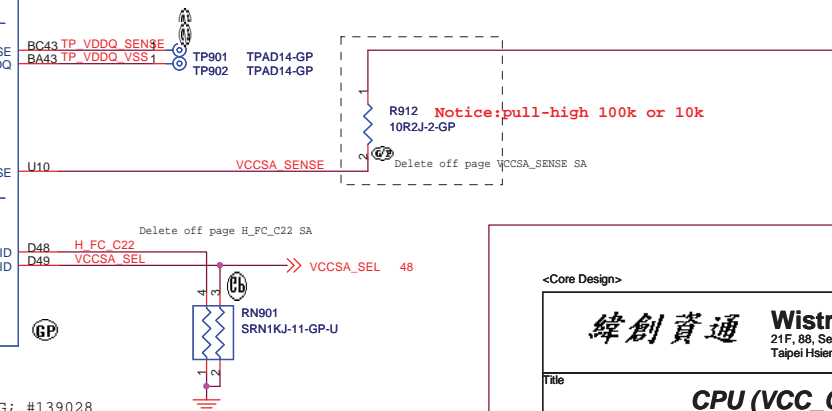


VDDQ Output Decoupling Recommendation:
1 x 330 uF 8 x 10uF (0603)
10 x 1 uF (0402)



PROCESSOR DDR 1.5V QUIET RAIL (BGA only)

+V1.5S_VCCD_Q should be short to +V1.5S_VCCDDQ on board



<Core Design>

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Title

CPU (VCC_GFXCORE)

Size

Document Number

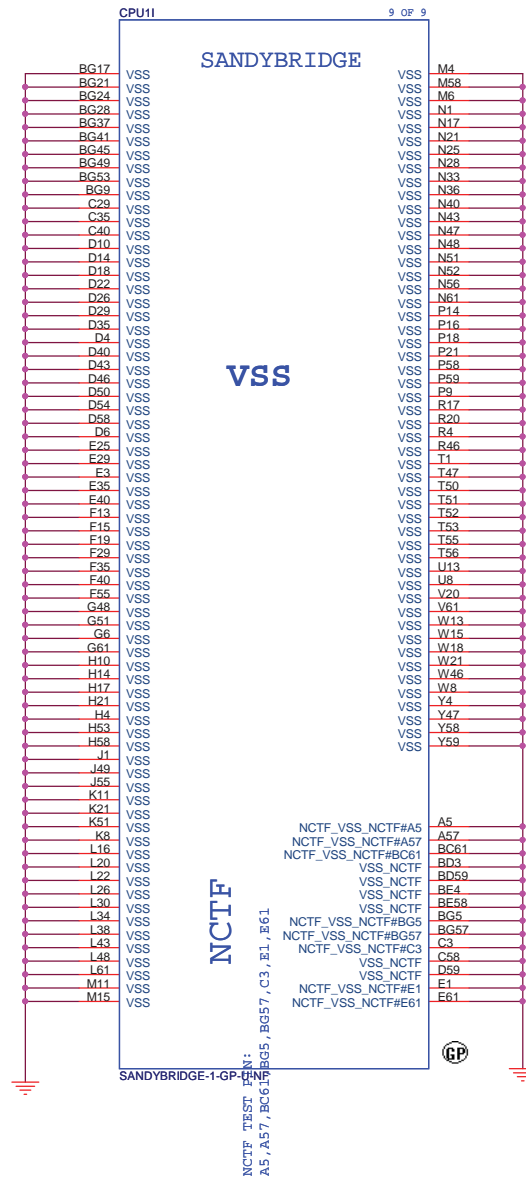
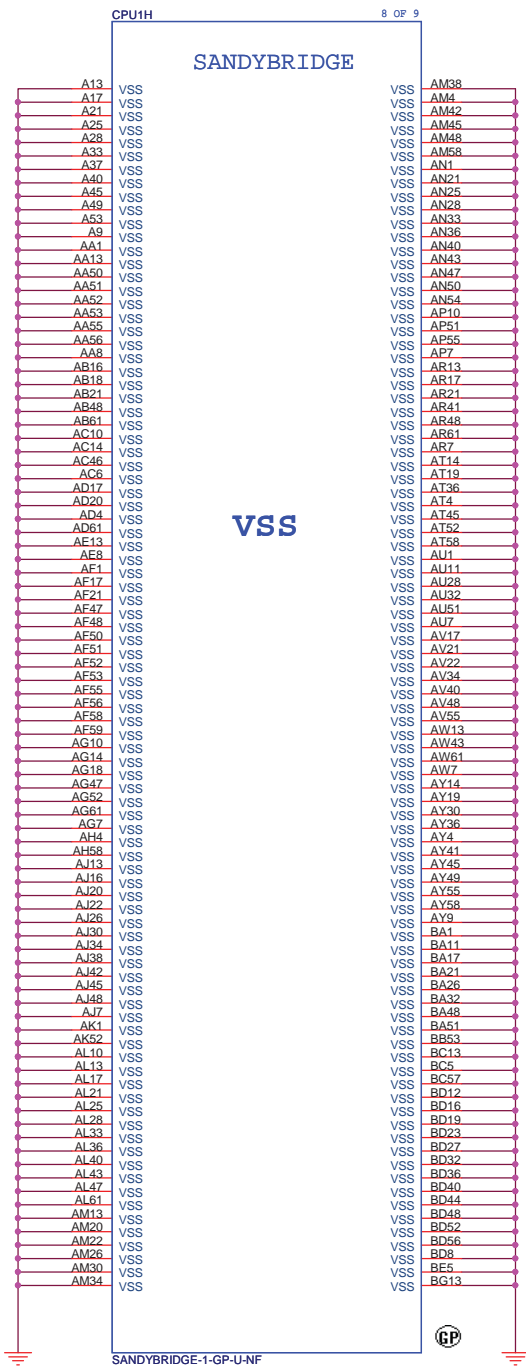
Hummingbird1_HR

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SSID = CPU



NCTF

NCTF_VSS_NCTF#A5
NCTF_VSS_NCTF#A57
NCTF_VSS_NCTF#BC61
VSS_NCTF
VSS_NCTF
VSS_NCTF
NCTF_VSS_NCTF#BG5
NCTF_VSS_NCTF#BG57
NCTF_VSS_NCTF#C3
VSS_NCTF
NCTF_VSS_NCTF#E1
NCTF_VSS_NCTF#E61

NCTF TEST PIN:
A5 ,A57 ,BG61 ,BG5 ,BG57 ,C3 ,E1 ,E61

Blanking

HR PX

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Title			
XDP			
Size	Document Number		Rev
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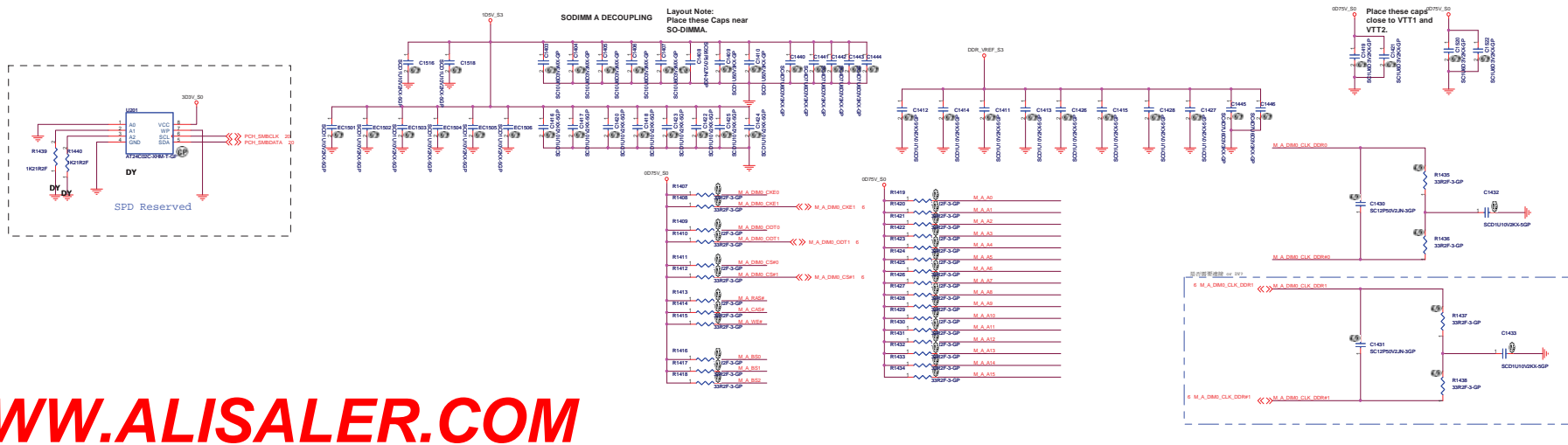
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Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>Hummingbird1 HR</div>	Rev <div>-2</div>
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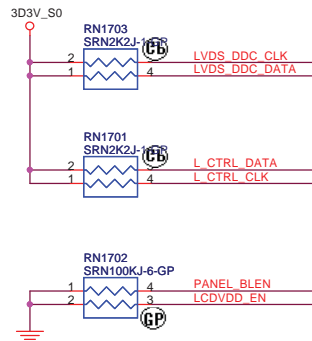
SSID = MEMORY

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HR PX		
<div>緯創資通Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
DDR3-SODIMM2		
Size	Document Number	Rev
Custom	Hummingbird1 HR	-2
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TitleDDR3-SODIMM2		
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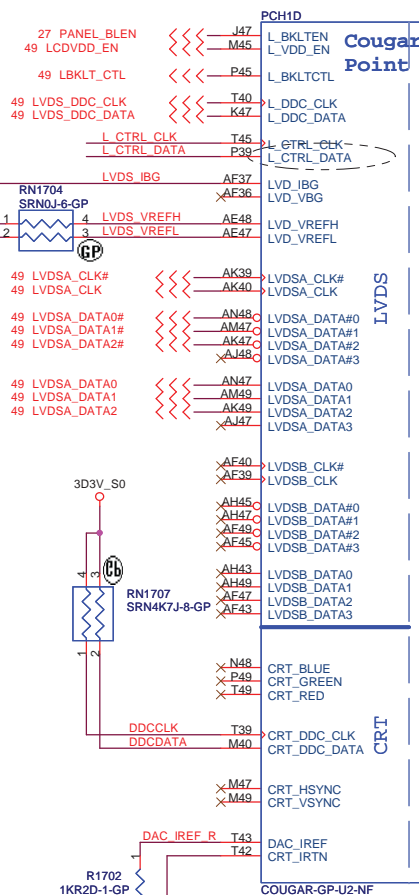
L_DDC_DATA(PAGE17):
This signal is on the LVDS interface.
This signal needs to be left NC if eDP is
used for the local flat panel display

Place near PCH

Impedance:90 ohm

Close to PCH side

Delete CRT pull down resistor

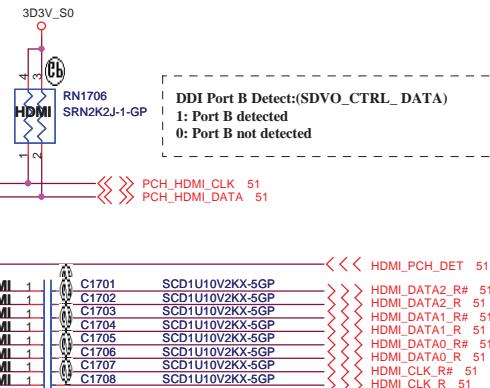


Digital Display Interface

Cougar Point

Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

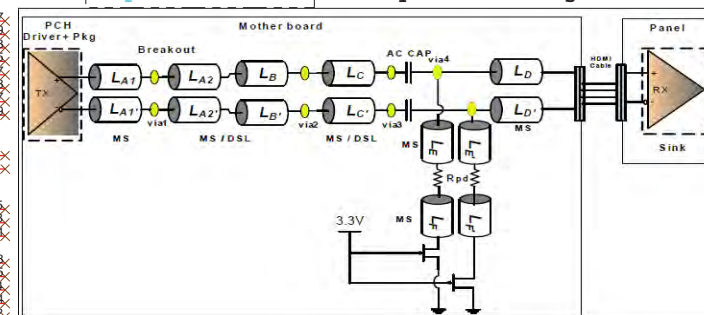
PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPDP	NA	DDPB_HPDP	HDMI_B_HPDP
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMI_B_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMI_B_CTRLDATA



DDI Port B Detect(SDVO_CTRL_DATA)
1: Port B detected
0: Port B not detected

Close to Connector side

Impedance:90 ohm TM request to change 85-ohm

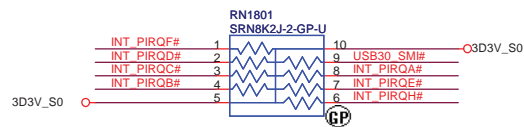


<Variant Name>

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Title: **PCH (LVDS/CRT/DDI)**
Size A3 Document Number: **Hummingbird1 HR** Rev: **-2**
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SSID = PCH



Al6 swap override Strap/Top-Block Swap Override jumper

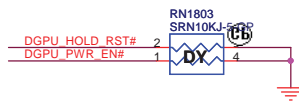
PCI_GNT#3 Low = Al6 swap override/Top-Block Swap Override enabled High = Default

BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

DGPU_HOLD_RST#

DGPU_PWR_EN#

DEBUG Card
PCH 71 CLK_PCL_LPC <<<
20 CLK_PCL_FB <<<
KBC 27 CLK_PCL_KBC <<<



INT_PIROA# K40
INT_PIROB# K38
INT_PIROC# H38
INT_PIRQD# G38

REQ1#/GPIO50
REQ2#/GPIO52
REQ3#/GPIO54
GNT1#/GPIO51
GNT2#/GPIO53
GNT3#/GPIO55

PIRQE#/GPIO2
PIRQF#/GPIO3
PIRQG#/GPIO4
PIRQH#/GPIO5

PME# K10
PLTRST# C6

CLKOUT_PCIO H49
CLKOUT_PC1 H43
CLKOUT_PC2 H48
CLKOUT_PC3 H42
CLKOUT_PC4 H40

OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)

Cougar Point

NVRAM

PCI

USB

COUGAR-GP-U2-NF

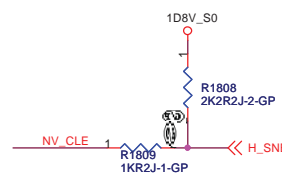
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DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

CRB : 2.2K

CEK1.T: 1K

Sandy Bridge / Ivy Bridge Processor
PROC_SELECT# connected to DF_TV5 via 1kΩ (MB) , via 4.7kΩ (DT).
DF_TV5 needs PU via 2.2kΩ to VccDFTERM



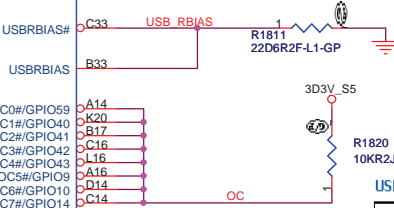
USB Ext. port 1 (HS)

External debug port use on Huron river platform

USB Table

Pair	Device
0	Touch Panel / 3G SIM(DY)
1	USB Ext. port 1 (HS)
2	Fingerprint(DY)
3	BLUETOOT
4	Mini Card2 (WWAN) (DY)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA / USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA(DY)
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card(DY)

USB_PN1 61
USB_PP1 61
USB_PN5 82
USB_PP5 82
USB_PN9 61
USB_PP9 61
USB_PN11 82
USB_PP11 82
USB_PN12 49
USB_PP12 49



USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title			
PCH (PCI/USB/NVRAM)			
Size A3	Document Number		Rev
	Hummingbird1 HR		-2
Date:	Tuesday, April 17, 2012	Sheet 18 of	102

4 DMI_RXN[3:0] << >>
4 DMI_RXP[3:0]

4 DMI_TXN[3:0] << >>
4 DMI_TXP[3:0]

PCH1C

3 OF 10

			FDI_TXN[7:0]	4
			FDI_TXP[7:0]	4

Deep S4/S5 **Not** Supported

RSMRST#

- 1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
- 2.DPWROK and RSMRST# will rise at the same time (connected on board)
- 3.SLP_SUS# and SUSACK# are left as 'no connect'
- 4.SUSWARN# used as SUSPWRDNACK/GPIO30

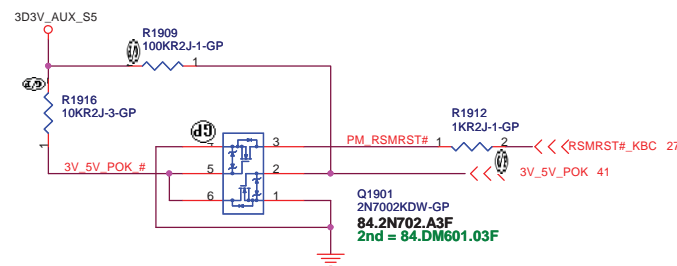


PM_RSMRST# C21 RSMRST#

```
PCIE_WAKE#
CRB : 1K
CEKLT: 10K
```

```
PM_RSMRST#
CPB : PL 1
ENIE : PL
```

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DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

RTC_AUX_

DSWODVREN

R1917 1

R1918 1 DY

330KR2J-L1-GP

330KR2J-L1-GP



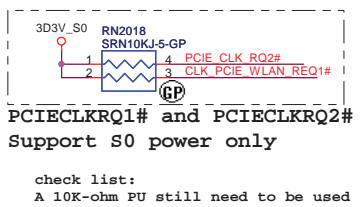
<Variant Names>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
PCH (DM I/FDI/PM)			
Size A3	Document Number		Rev
	Hummingbird1 HR		-2
Date	Tuesday, April 17, 2012		Sheet 19 of 102

SSID = PCH

USB3.0 CLK

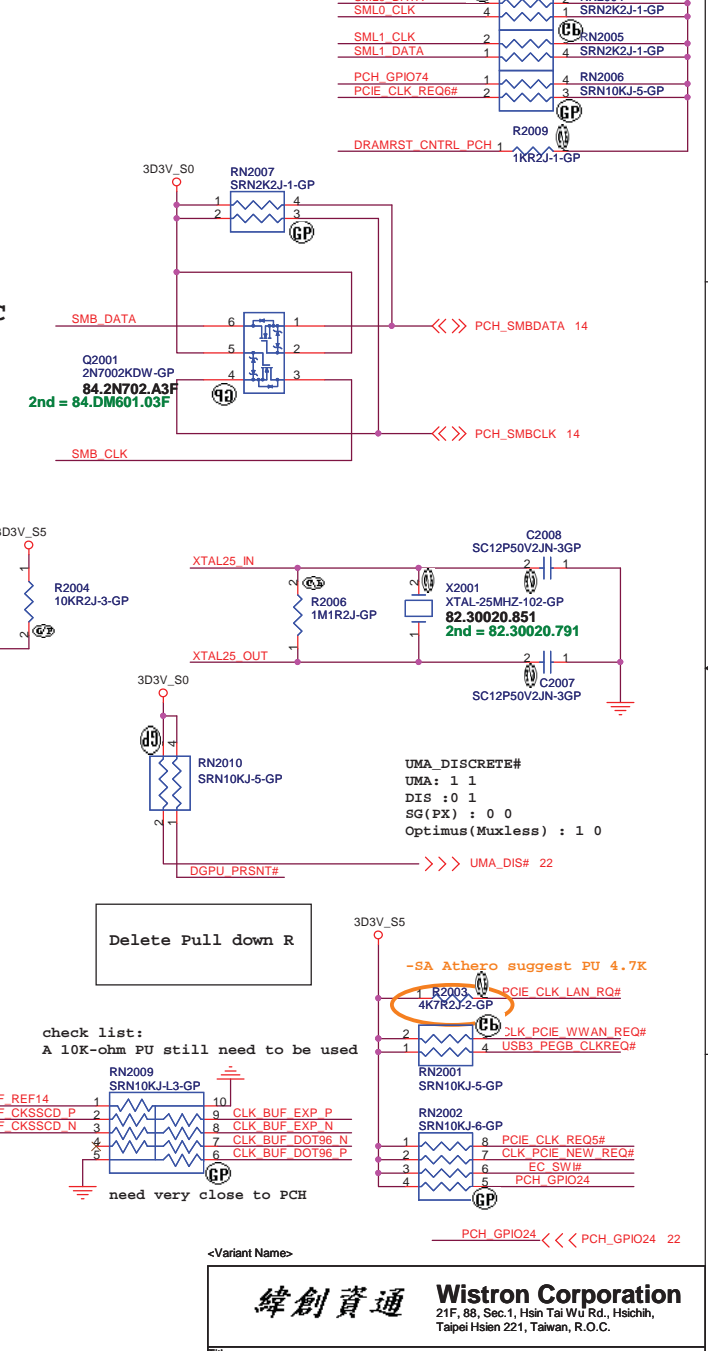
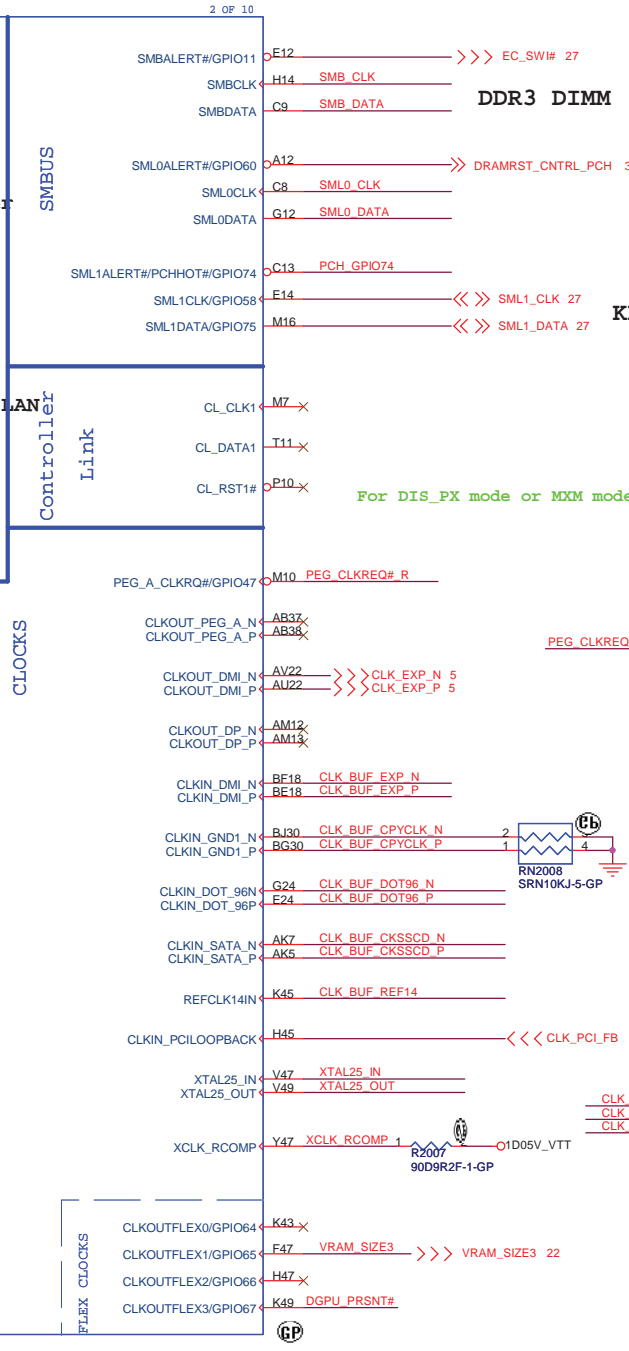
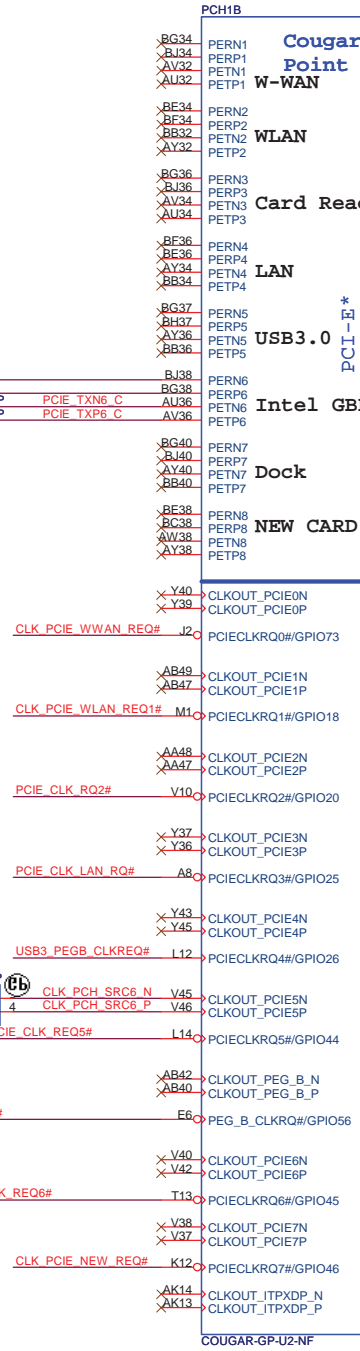


82 PCIE_RXN6
82 PCIE_RXP6
82 PCIE_TXN6
82 PCIE_TXP6

WWAN CLK

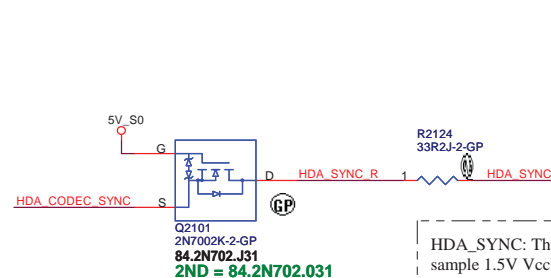
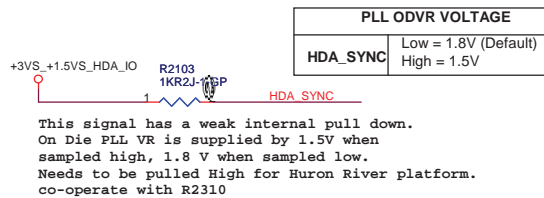
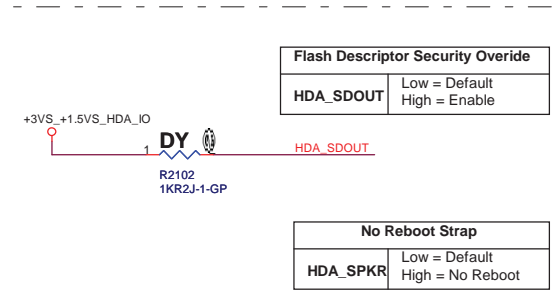
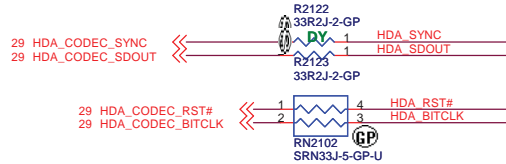
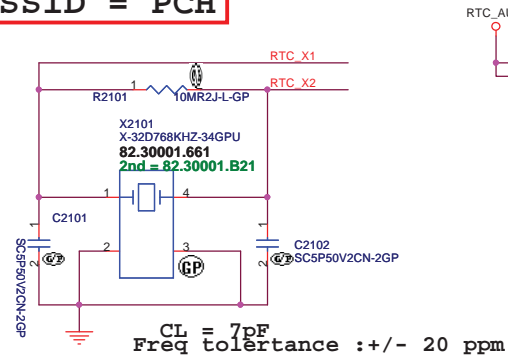
WLAN CLK

82 CLK_PCIE_WLAN#
82 CLK_PCIE_WLAN
82 CLK_PCIE_WLAN_REQ#

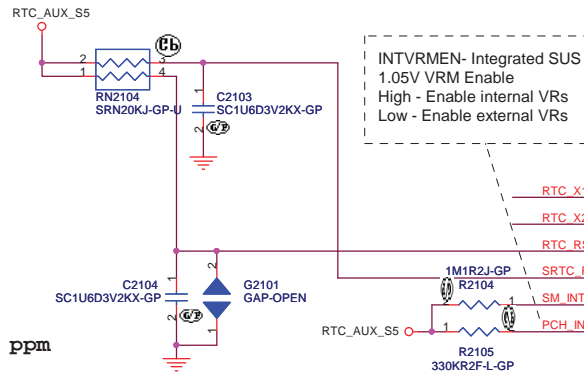


Prioritize 27/14/24/48/25-MHz FLEX on FLEX1 and FLEX3
- Do not change 27/14/24/48/25-MHz FLEX clock on FLEX0 and FLEX2
if for 14/25 MHz PCI clocks + PCI loopback are routed.

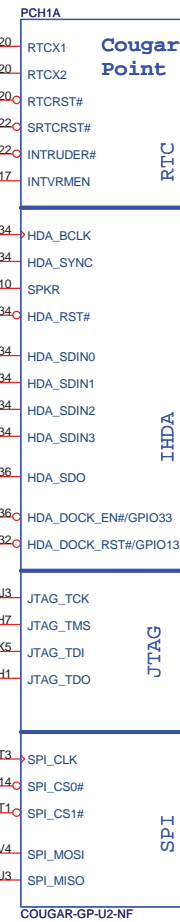
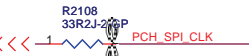
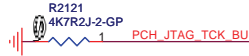
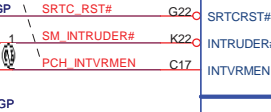
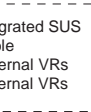
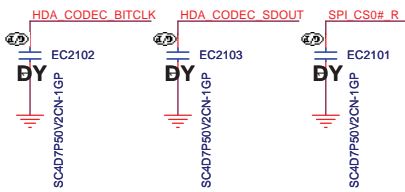
SSID = PCH



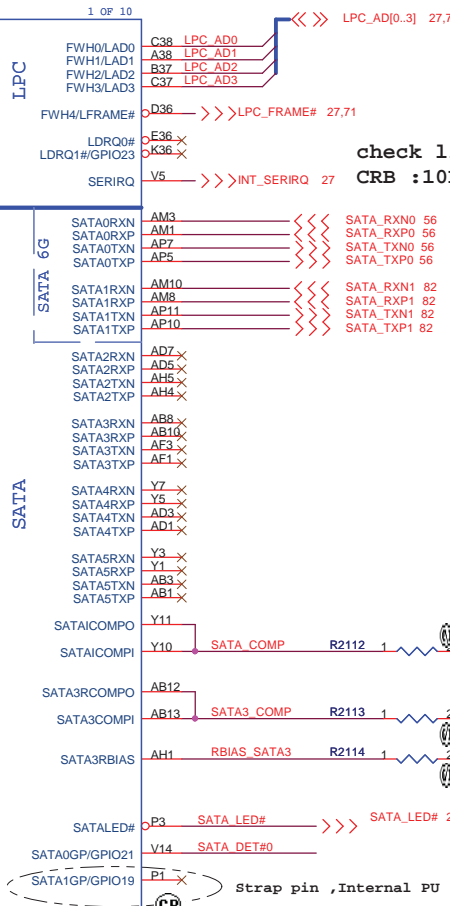
HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.



RTC Reset



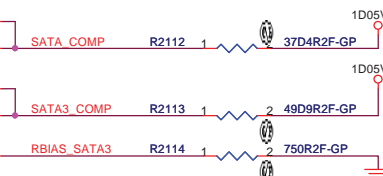
71.COUGA.00U



```
check list:8.2K PU
CRB :10K PU
```

HDD1

M-SATA



Strap pin ,Internal PU



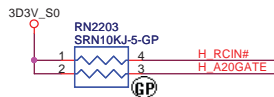
<Variant Name>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title			
PCH (SPI/RTC/LPC/SATA/IHDA)			
Size	Document Number	Rev	
A3	Hummingbird1 HR	-2	
Date:	Tuesday, April 17, 2012	Sheet	21 of 102

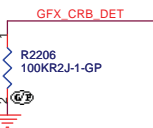
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Note:
For PCH debug with XDP, need to NO STUFF R2218



check list:
if are unused, PU or PD TPAD14-GP TP2204

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY



3D3

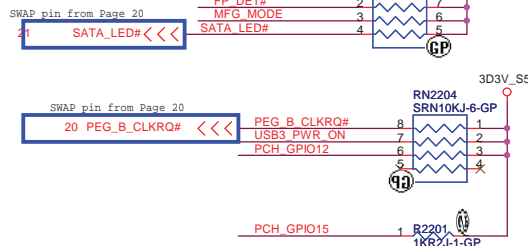
EC SMI#		1		8	
EC SCI#		2		7	
DGPU_HPD_INTR#		2		6	
		3	5		

⚡

Ⓟ

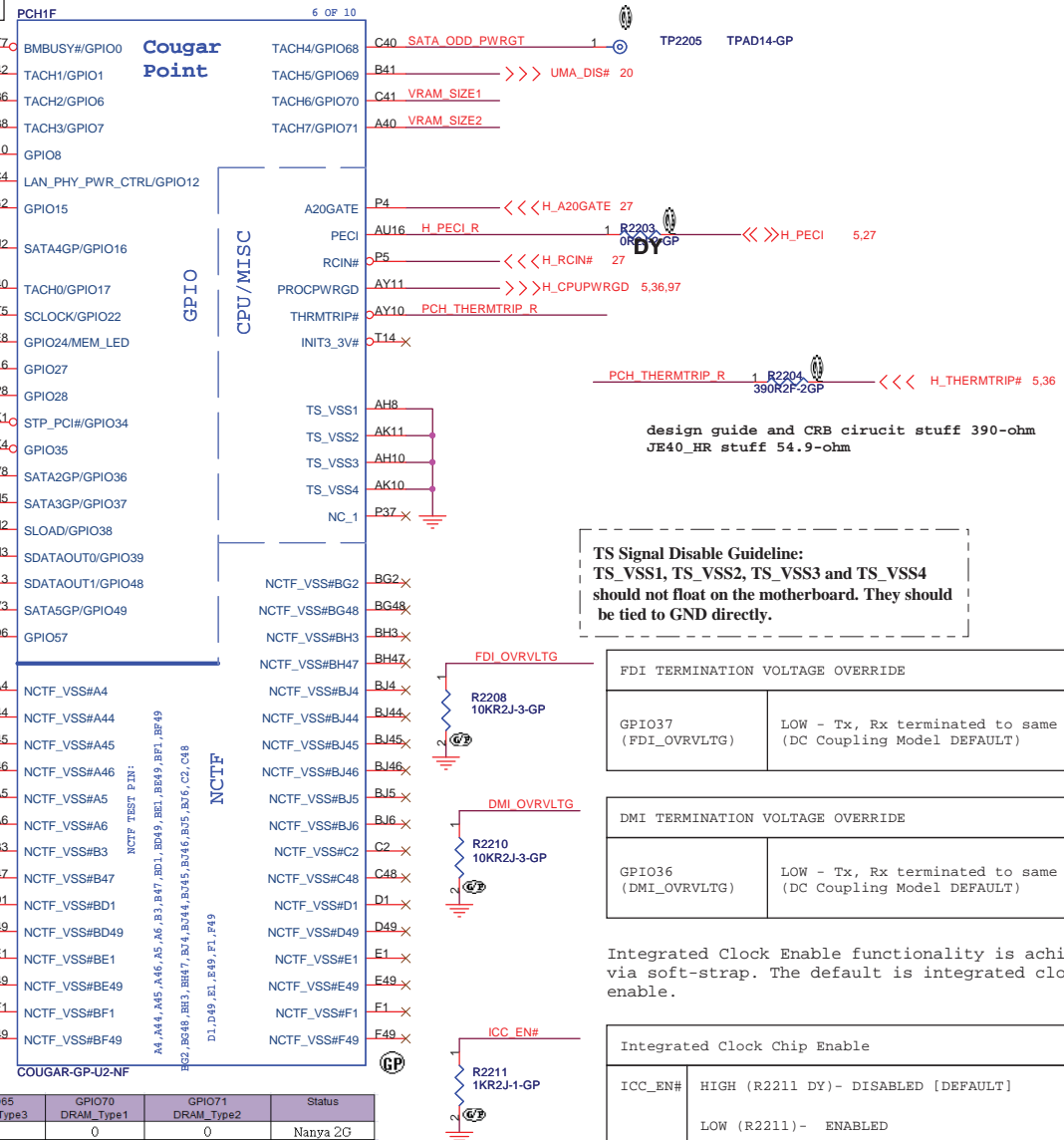
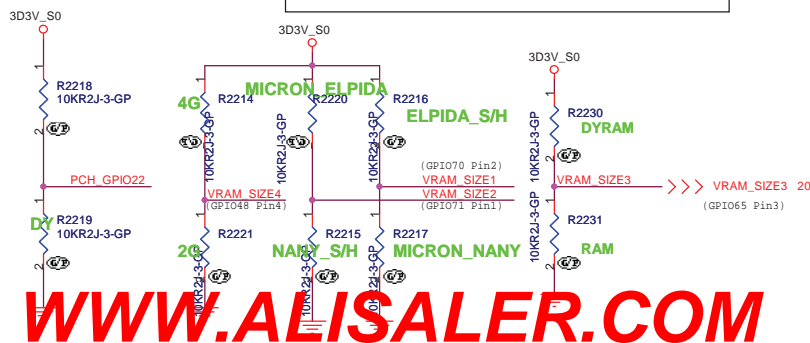
PSW CLR#		1		8	
FP DET#		2		7	
MFG MODE		3		6	
SATA_LED#		4		5	

Ⓟ



Pull high: 800MHZ
Pull low :900MHZ

NOTE: This signal has a weak internal pull-up 20K
 ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT
 DISABLED -- LOW (R2212 STUFFED)



TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLGTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLGTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved
via soft-strap. The default is integrated clock
enable.

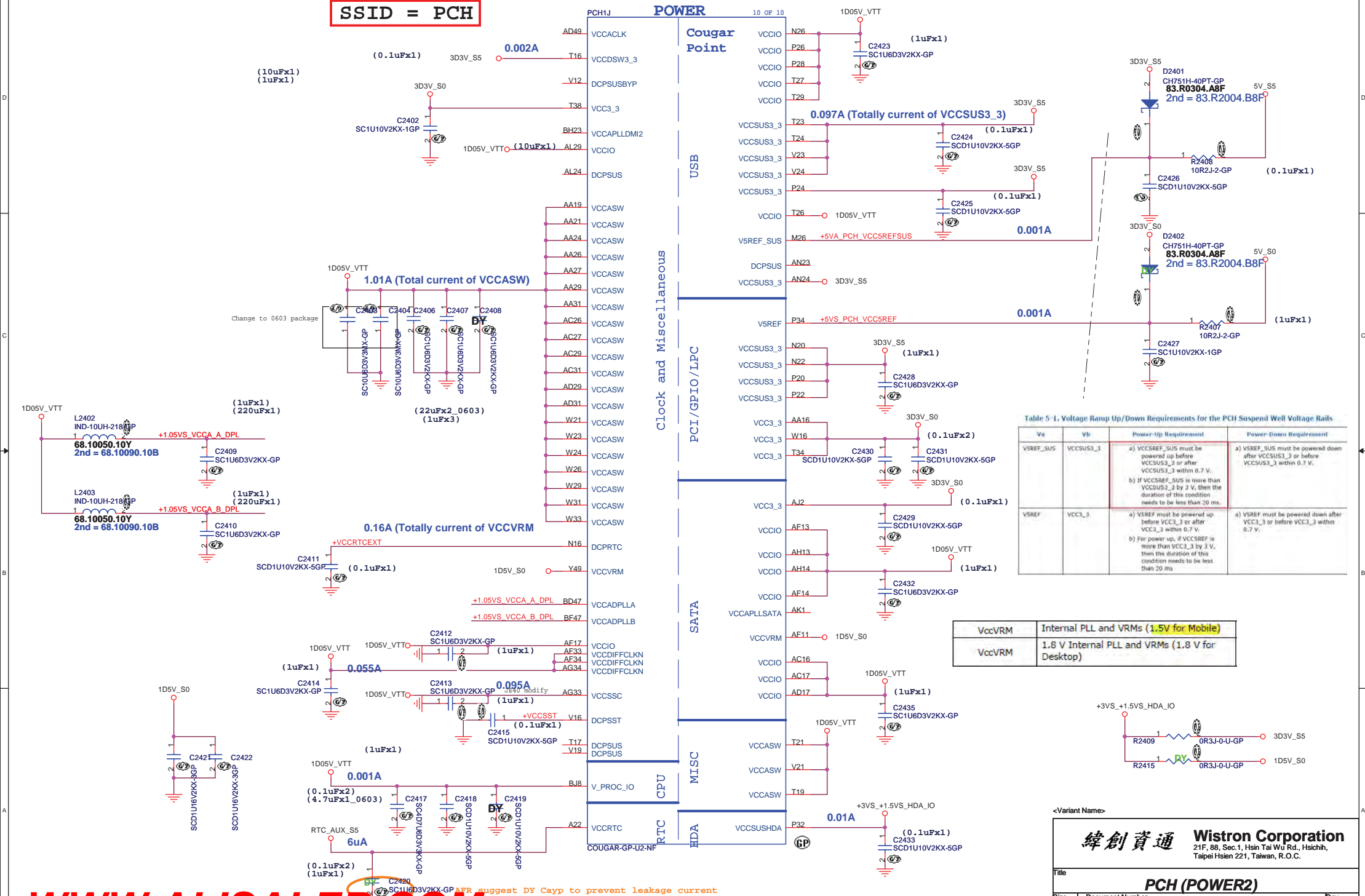
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
PCH (GPIO/CPU)			
Size A3	Document Number		Rev
	Hummingbird1 HR		-2
Date:	Tuesday, April 17, 2012	Sheet 22 of	102

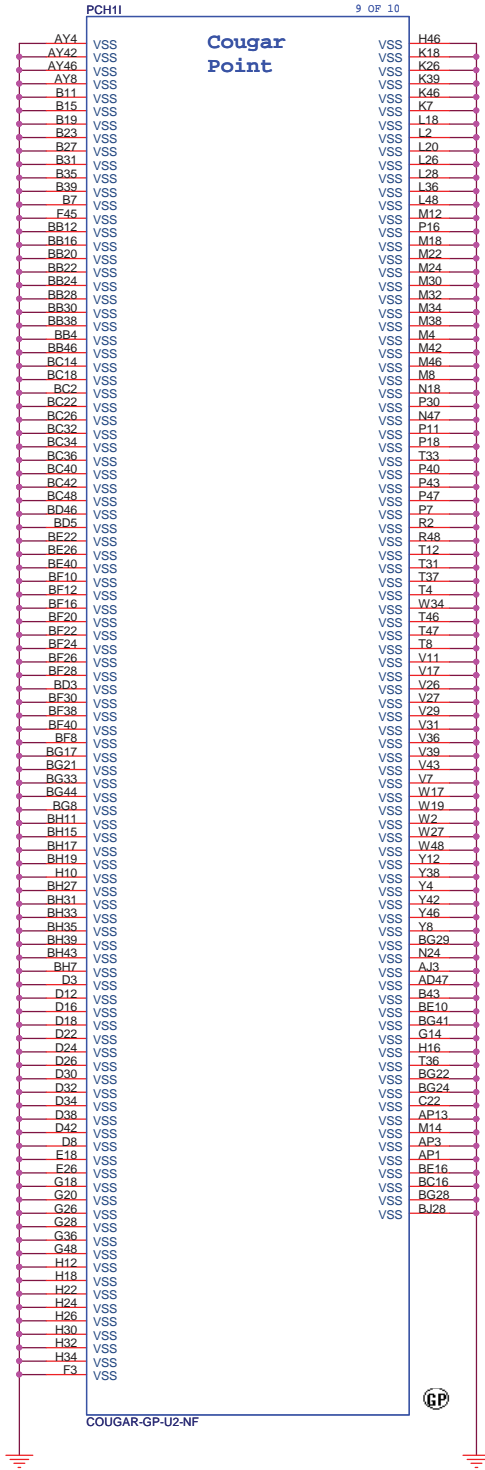
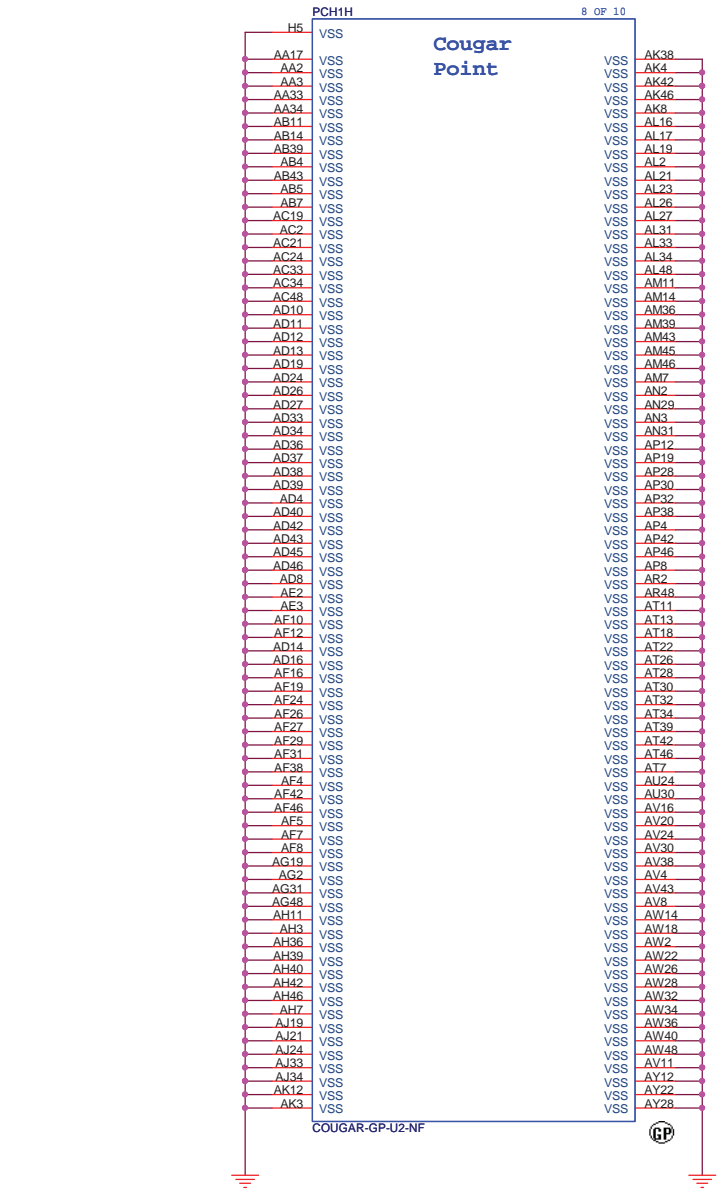
GPI048 DRAM_Type4	GPI055 DRAM_Type3	GPI070 DRAM_Type1	GPI071 DRAM_Type2	Status
0	0	0	0	Nanya 2G
0	0	0	1	Micron 2G
0	0	1	0	HYNIX 2G
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	Nanya 4G
1	0	0	1	Micron 4G
1	0	1	0	Samsung 4G
1	0	1	1	ELPIDA 4G
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

SSID = PCH



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SSID = PCH



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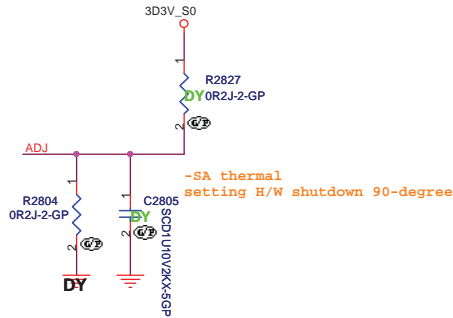
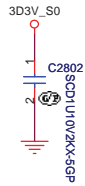
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<Variant Name>

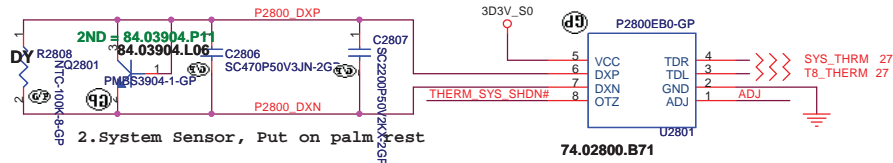
<div>緯創資通Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
Clock(colay)		
Size	Document Number	Rev
A4	Hummingbird1	HR-2
Date: Tuesday, April 17, 2012		Sheet 26 of 102

SSID = Thermal

Thermal sensor P2800

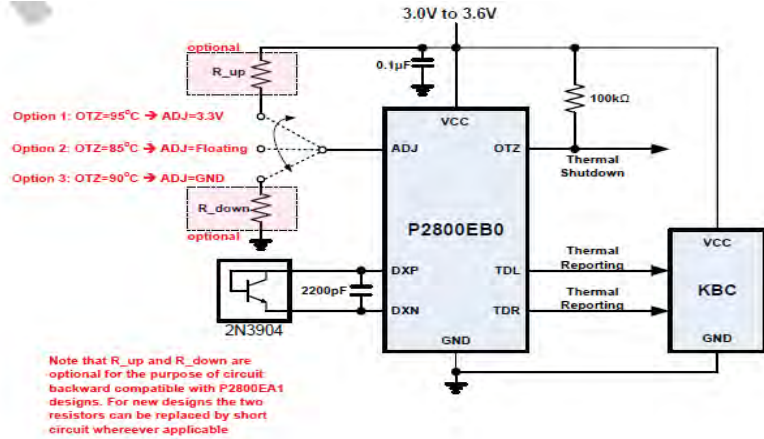


Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.

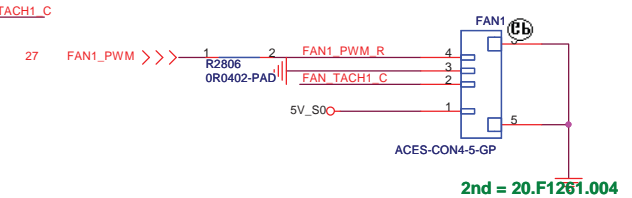
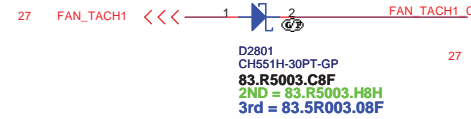
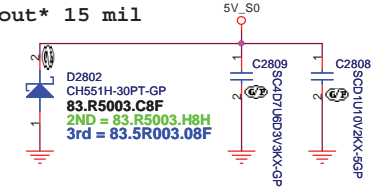


[Rev B]

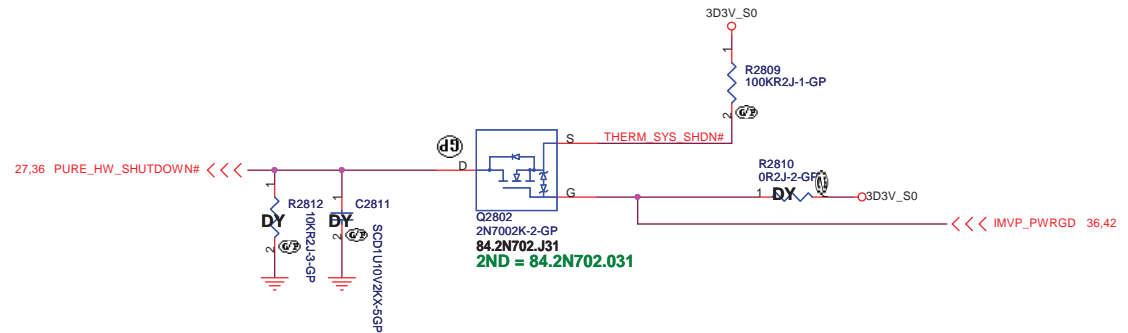
1.H/W T8 Shutdown



Layout 15 mil



For PWM FAN

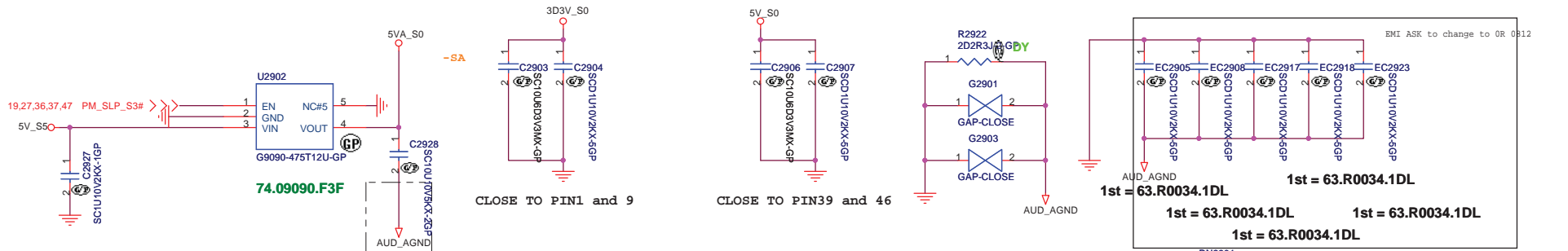


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HR PX

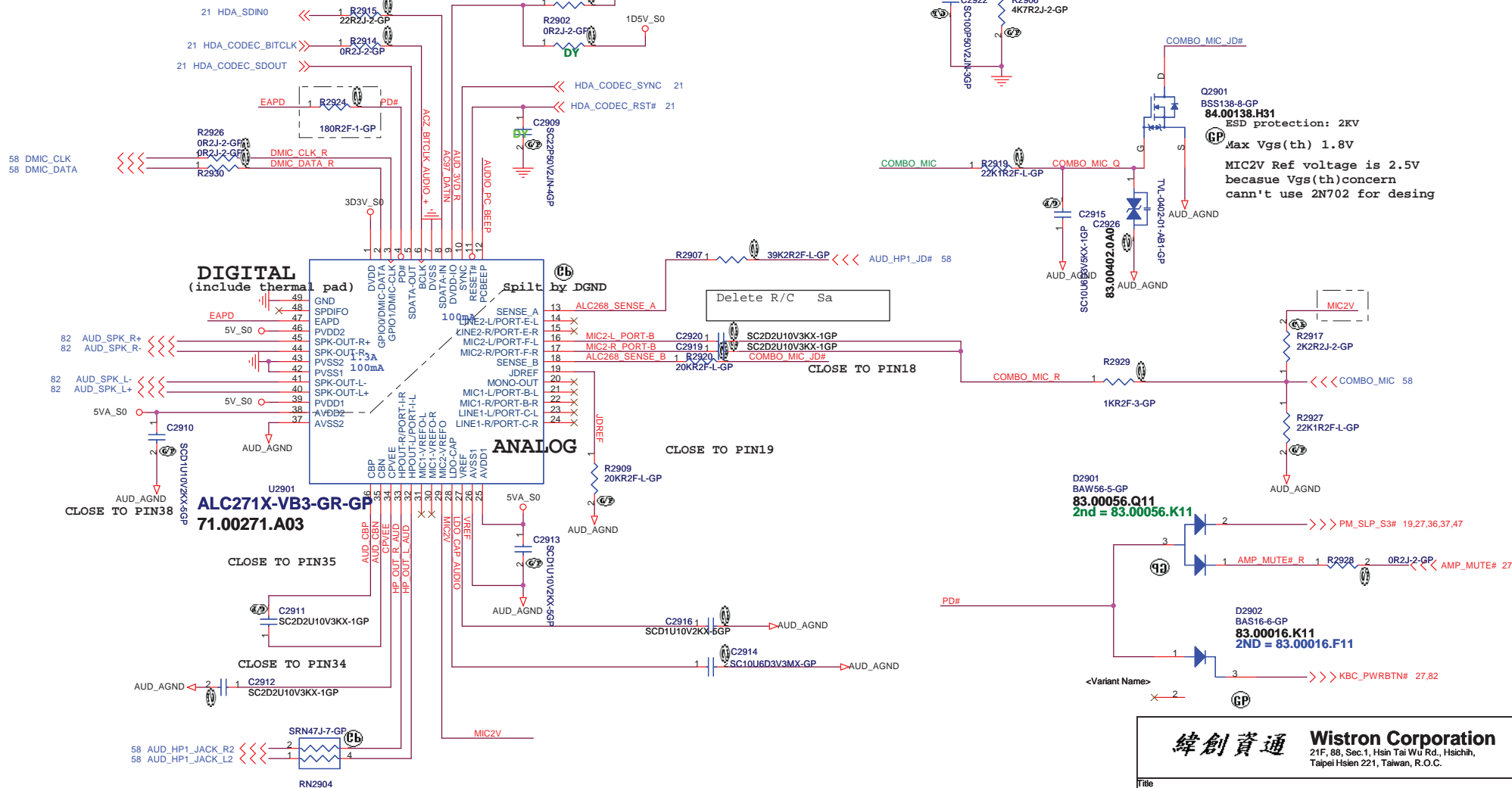
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Thermal P2800/Fan Controller P2793		
Size A3	Document Number	Rev
Hummingbird1 HR		-2
Date: Tuesday, April 17, 2012	Sheet 28	of 102



if use LDO, have to PVDD have been ramp up after AVDD, if not, might occur issue

PM_SLP_S3# driver strength is insufficient, if no stuff, waveform will abnormally when S3 mode



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<Variant Name>		
<div>緯創資通Wistron Corporation21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Audio AMP</div>		
Size <div>A4</div>	Document Number <div>Hummingbird1 HR</div>	Rev <div>-2</div>
Date <div>Tuesday, April 17, 2012</div>		Sheet <div>30</div> of <div>102</div>

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<Variant Name>

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
AR8158			
Size	Document Number		Rev
A3	Hummingbird1 HR		-2
Date:	Tuesday, April 17, 2012		Sheet 31 of 102

Card reader move to small board

<Variant Name>		
<div>緯創資通Wistron Corporation21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>RTS5159 (CARD READER)</div>		
Size <div>A4</div>	Document Number <div>Hummingbird1 HR</div>	Rev <div>-2</div>
Date: Tuesday, April 17, 2012		Sheet 32 of 102

(Blanking)

<Variant Name>

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>Hummingbird1 HR</div>	Rev <div>-2</div>
Date: Tuesday, April 17, 2012		Sheet 33 of 102

(Blanking)

<Variant Name>		
<div>緯創資通Wistron Corporation21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
TitleReserved		
SizeA4	Document NumberHummingbird1 HR	Rev-2
Date: Tuesday, April 17, 2012		Sheet 34 of 102

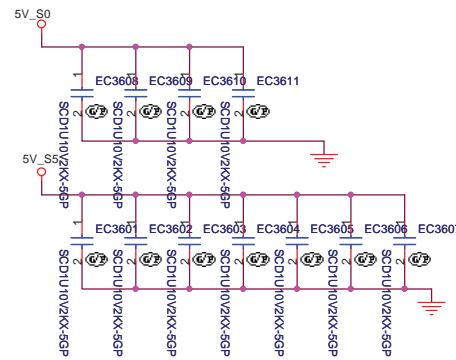
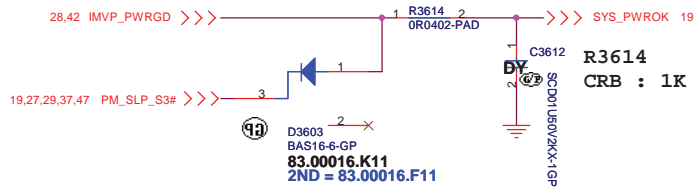
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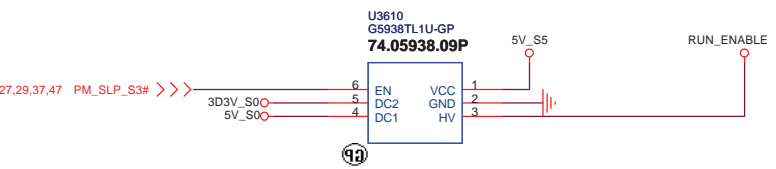
HR PX

Title	
USB 3.0 Controller	
Size A3	Document Number Hummingbird1 HR
Date: Tuesday, April 17, 2012	Sheet 35 of 102

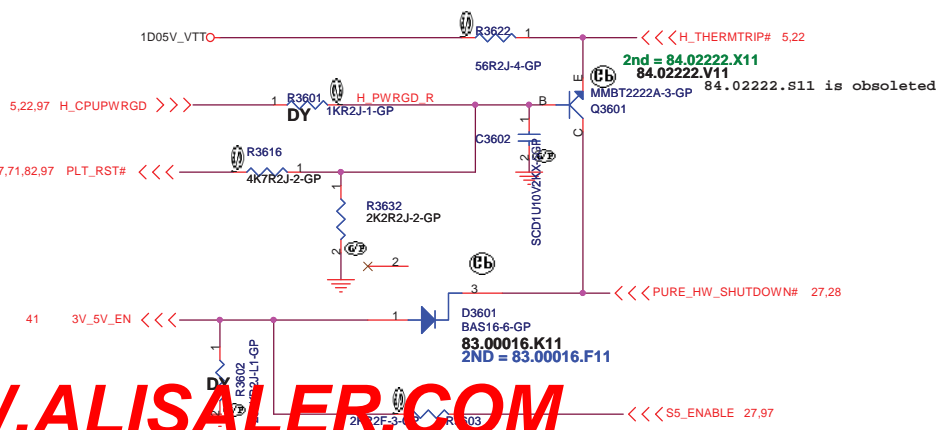
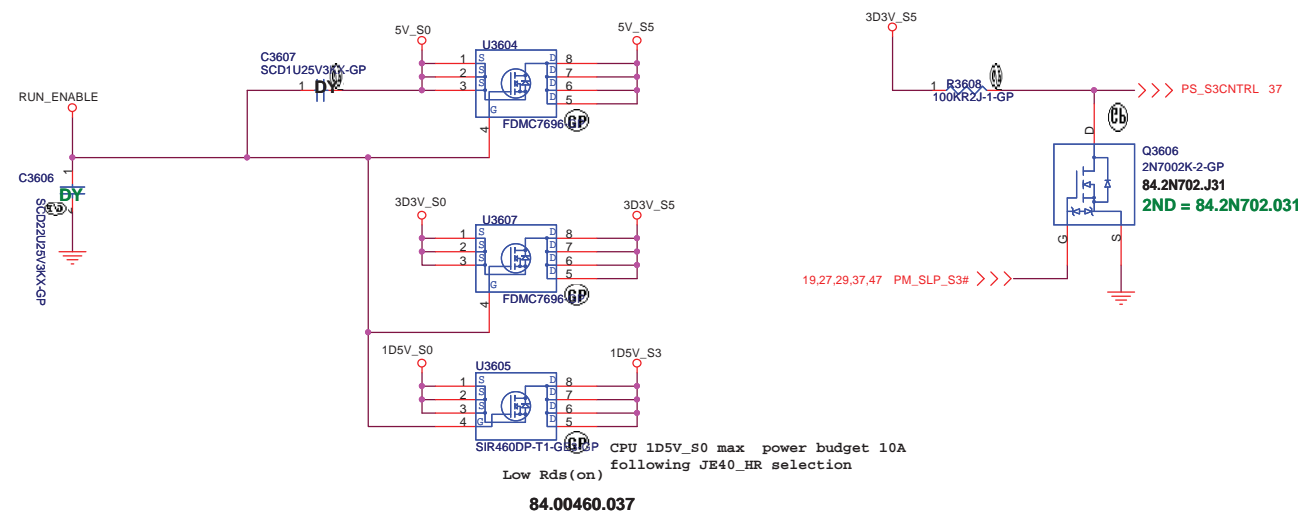
Power Sequence



ANNIE Run Power

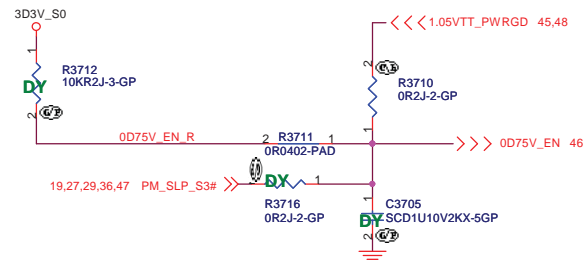
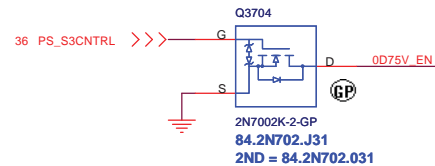
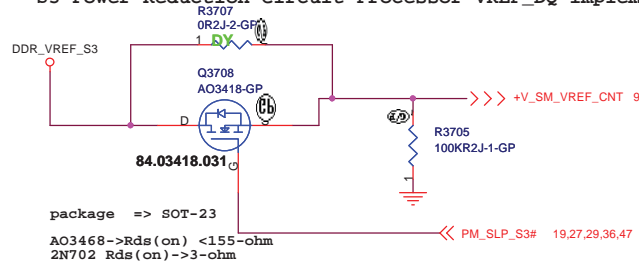


Modify the MOS package for placement

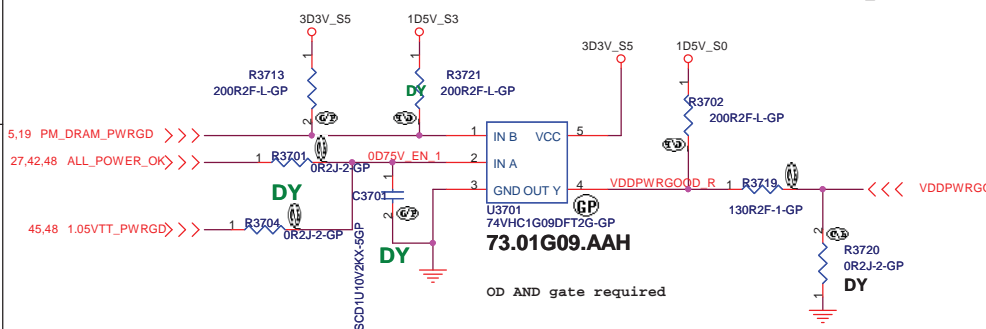


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Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation

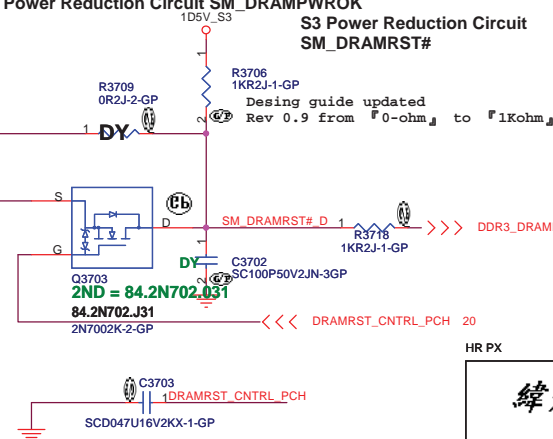


Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK

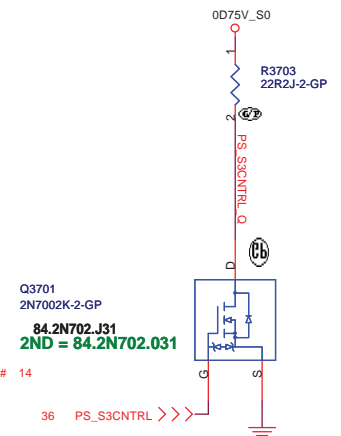


For U3701 not OD AND gate
R3719 to 64.15015.6DL
R3720 to 64.75005.6DL
R3702 to DY

Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK
S3 Power Reduction Circuit SM_DRAMRST#



Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



HR PX

Title		Wistron Corporation	
Size A3		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Document Number		ADAPTER	
Date: Tuesday, April 17, 2012		Hummingbird1 HR	
Sheet 37 of 102		Rev -2	

Move to small board

HR PX

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>DCIN JACK</div>		
Size <div>A4</div>	Document Number <div>Hummingbird1 HR</div>	Rev <div>-2</div>
Date <div>Tuesday, April 17, 2012</div>		Sheet <div>38</div> of <div>102</div>

Move to small board

<Variant Name>

<div>緯創資通Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
BATT CONN		
Size	Document Number	Rev
A4	Hummingbird1	HR-2
Date: Tuesday, April 17, 2012		Sheet 39 of 102

Move to small board

<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CHARGER BQ24745

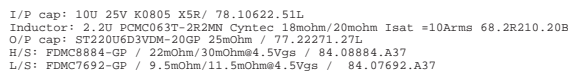
Size
A3

Document Number
Hummingbird1 HR

Rev
-2

Date: Tuesday, April 17, 2012

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I/P cap:10U 25V K0805 X5R/ 78.10622.51L
Inductor: 1.50UH PCMC104T-1R5 Cyntec 3.8mohm/4.2mohm Isat =33Arms
O/P cap: ST220U6D3VDM-20GP 25mOhm / 77.22271.27L
H/S: SIR172DP-T1-GE3-GP / 10.3mOhm/12.4mOhm@4.5Vgs / 84.00172.037
L/S: SIR460DP-T1-GE3-GP / 4.9mOhm/6.1mOhm@4.5Vgs / 84.00460.037

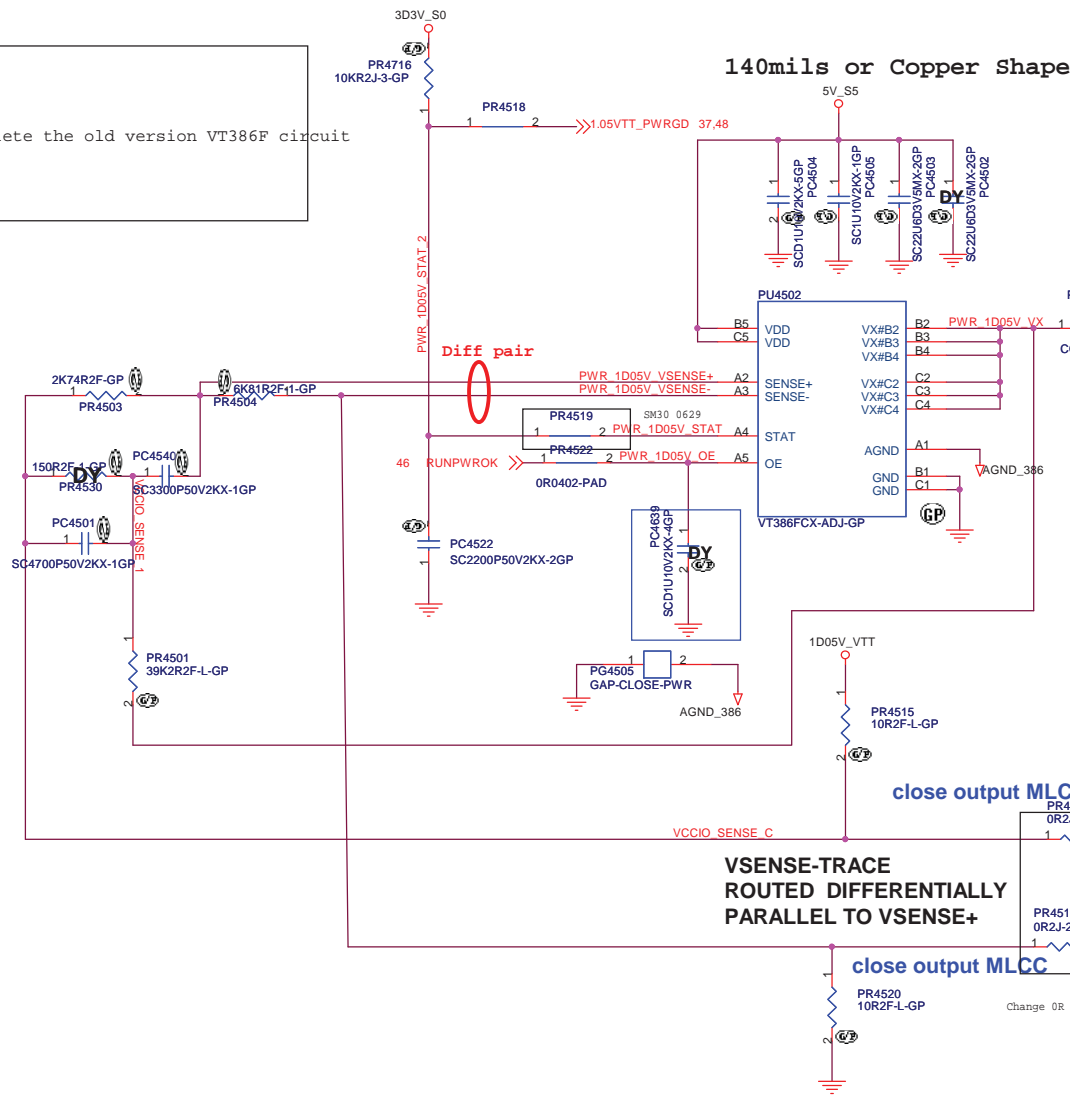
TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3	365kHz	460kHz
VREG5	365kHz	460kHz



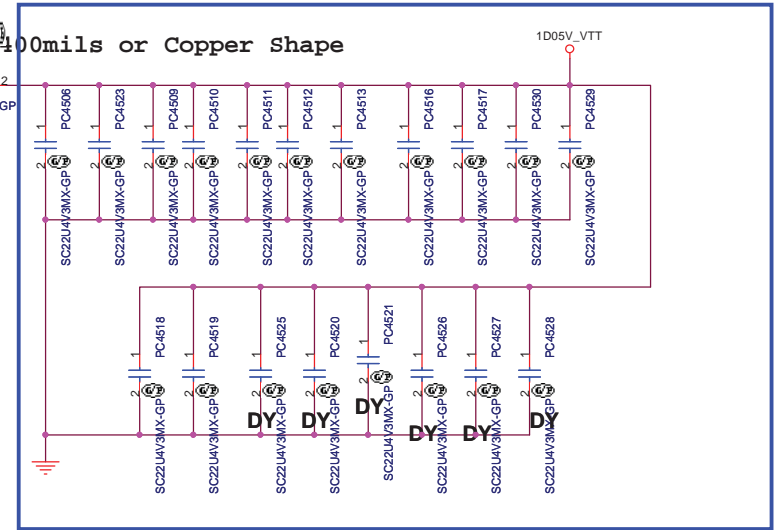
WWW.ALISALER.COM



Delete the old version VT386F circuit



Design Current = 12A
15.6A < OCP < 17.7A



Change to 0603_4V

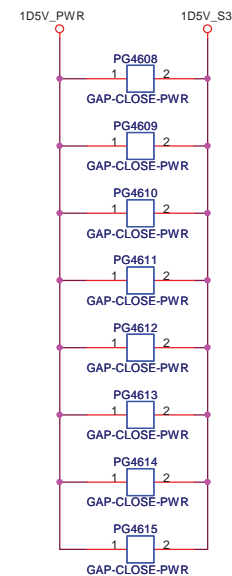
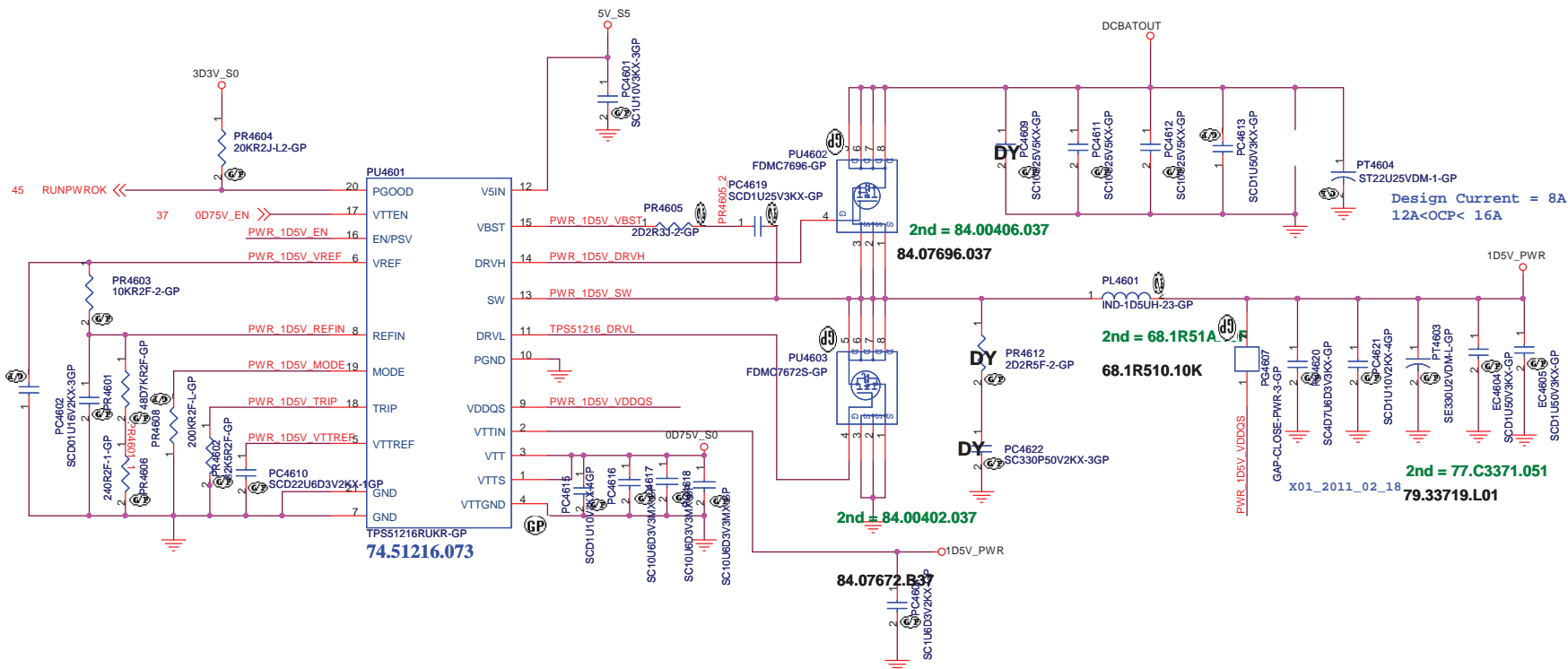
VSENSE-TRACE
ROUTED DIFFERENTIALLY
PARALLEL TO VSENSE+

close output MLCC

Change 0R PAD to 0R and DY

<Variant Name>

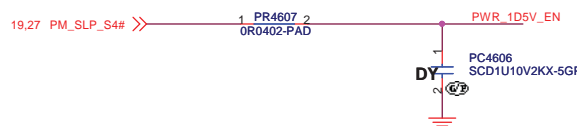
SSID = PWR.Plane.Regulator 1p5v0p75v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

PR5003	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: IND-1D5UH-23-GP 14mohm/15mohm Isat =18Arms 68.1R510.10K
O/P cap: SE330U2VDM-L-GP 9mOhm / 79.33719.L01
H/S: SIS412DN-T1-GE3-GP / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S: SI7716ADN-T1-GE3-GP / 13.5mOhm/16.5mOhm@4.5Vgs / 84.07716.037



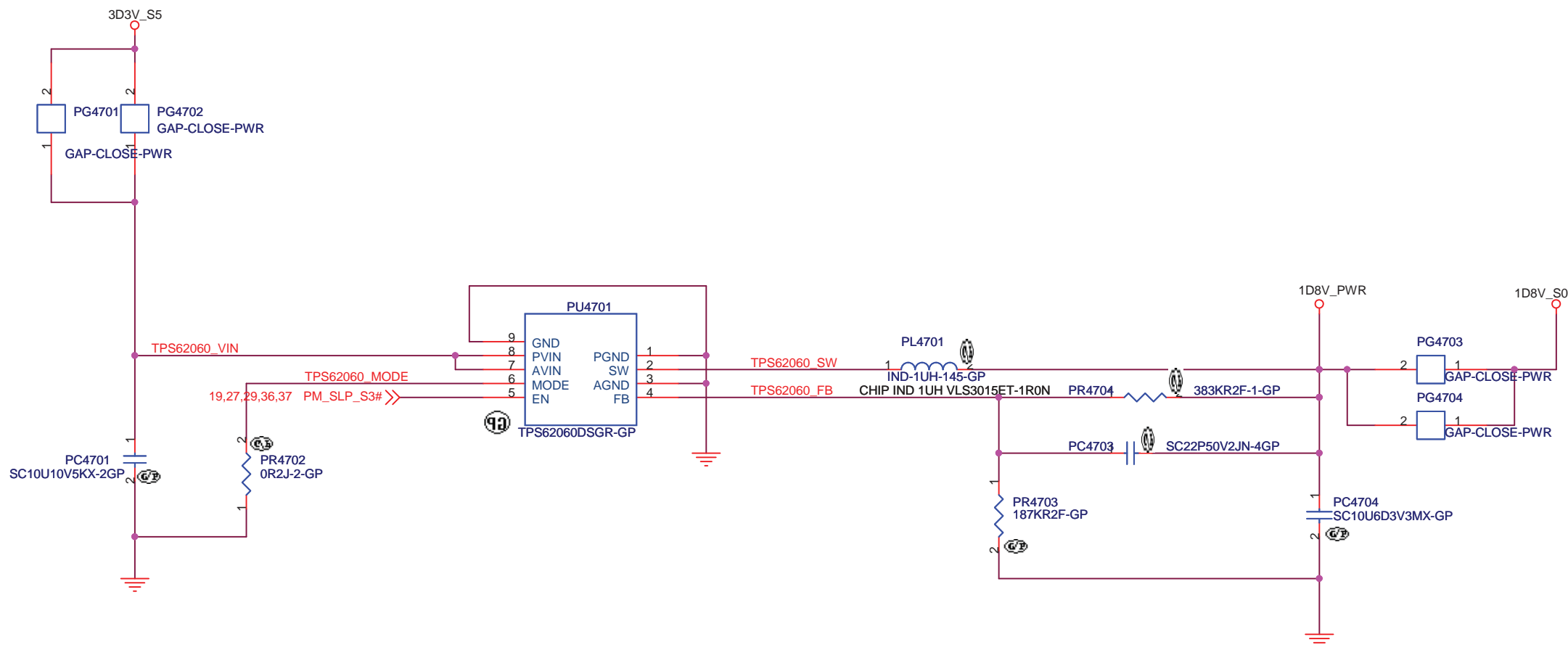
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
TPS51116 +1.5V SUS			
Size A3	Document Number		Rev
	Hummingbird1 HR		-2
Date:	Tuesday, April 17, 2012	Sheet 46 of	102

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```
SSID = PWR.Plane.Regulator_1p8v
```



<Variant Name>

緯創資通

Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title	DC CONVERTER 1D8V
-------	--------------------------

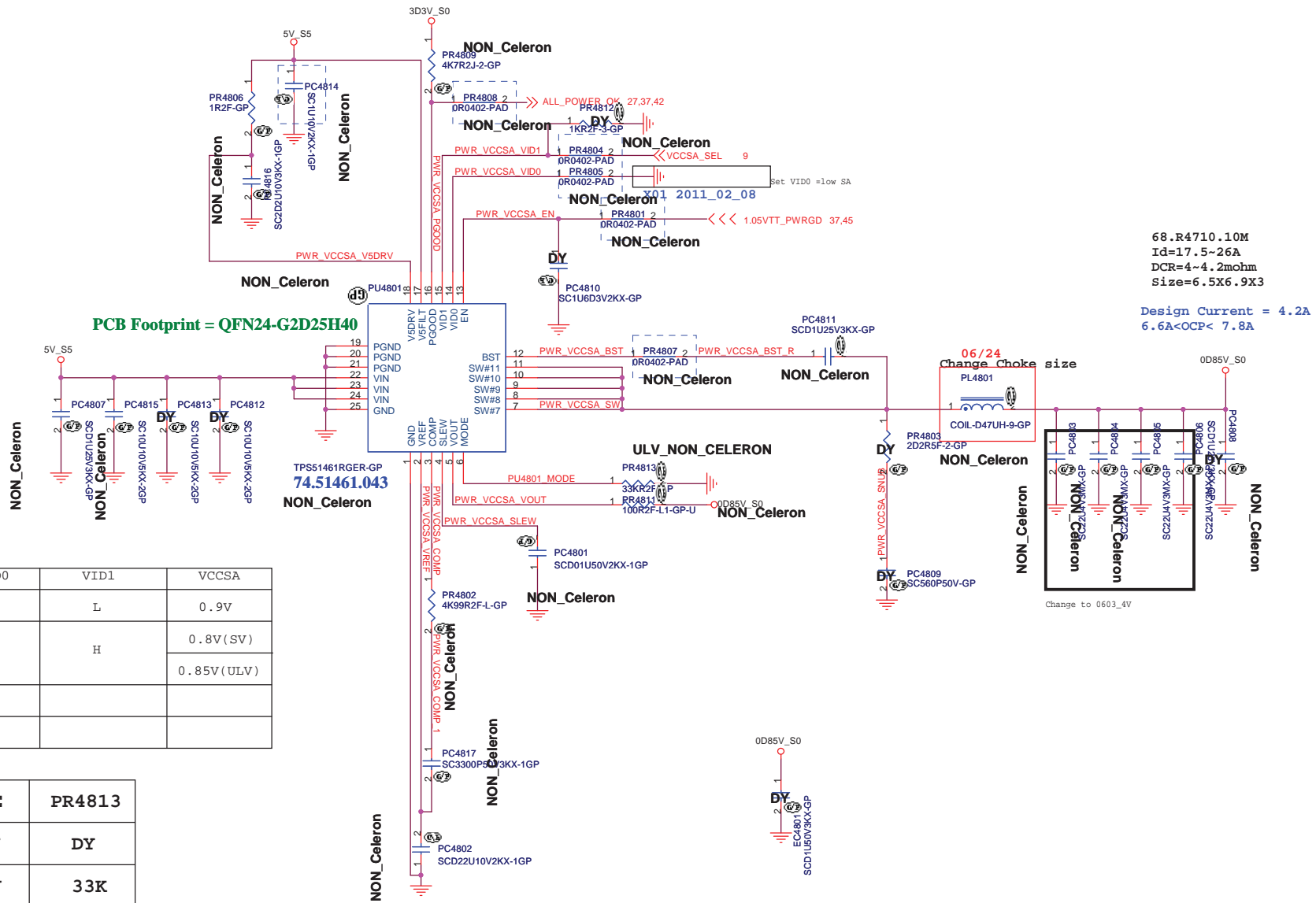
Size	Document Number	Rev
------	-----------------	-----

A4	Hummingbird1 HR	-2
----	-----------------	----

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TPS51461 for VCCSA



VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V(SV)
		0.85V(ULV)

TYPE	PR4813
SV	DY
ULV	33K

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<Variant Name>

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title	TPS51461_VCCSA
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Size A3	Document Number
Date: Tuesday, April 17, 2012	

Hummingbird1 HR	Rev -2
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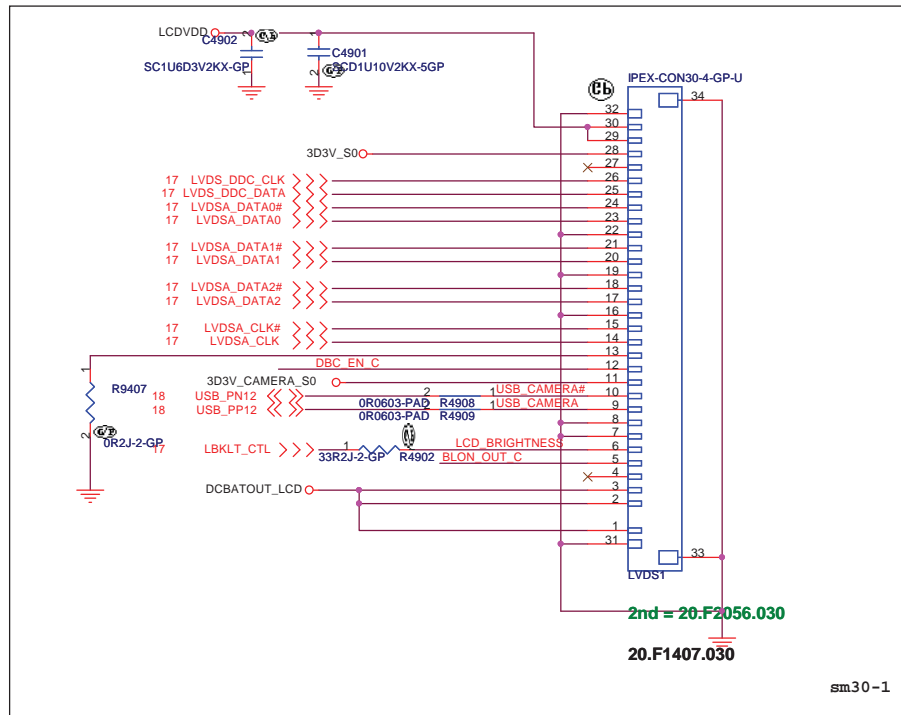
Rev
-2

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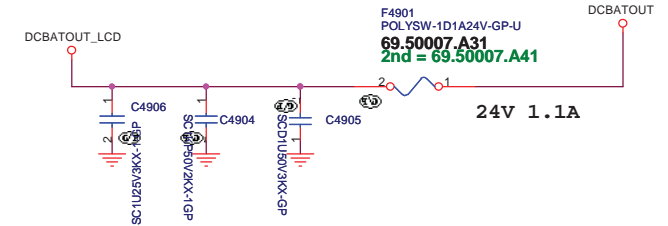
SSID = VIDEO

Reverse the pin define because of cable issue

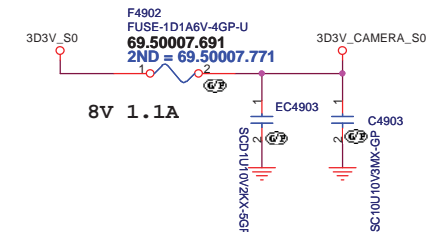
LVDS CONNECTOR



INVERTER POWER

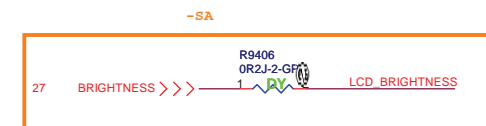
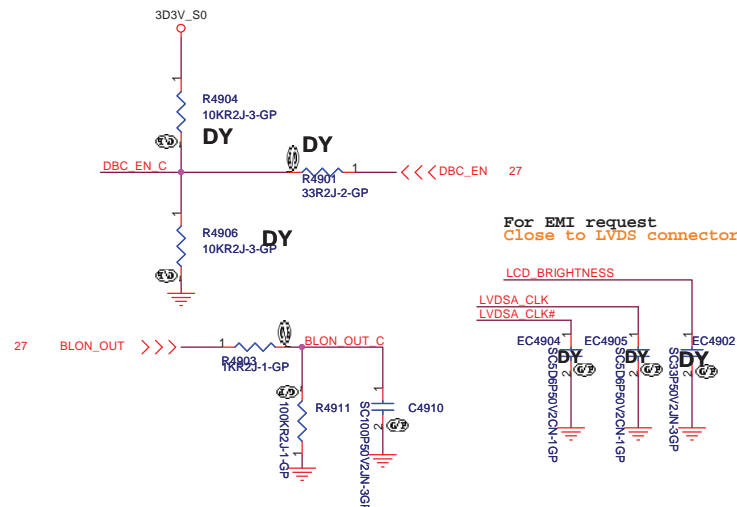
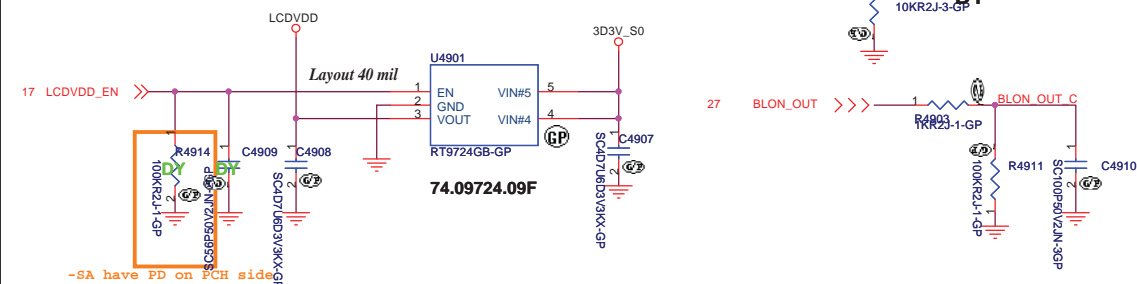


Camera Power



SSID = VIDEO

LCD POWER for ANNIE



<Variant Name>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

LCD Connector		
Size A3	Document Number	Rev
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Pull High 5V Design on CRT Board
CRT DDCDATA & DDCCLK level shift

<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CRT Connector

Size
A3

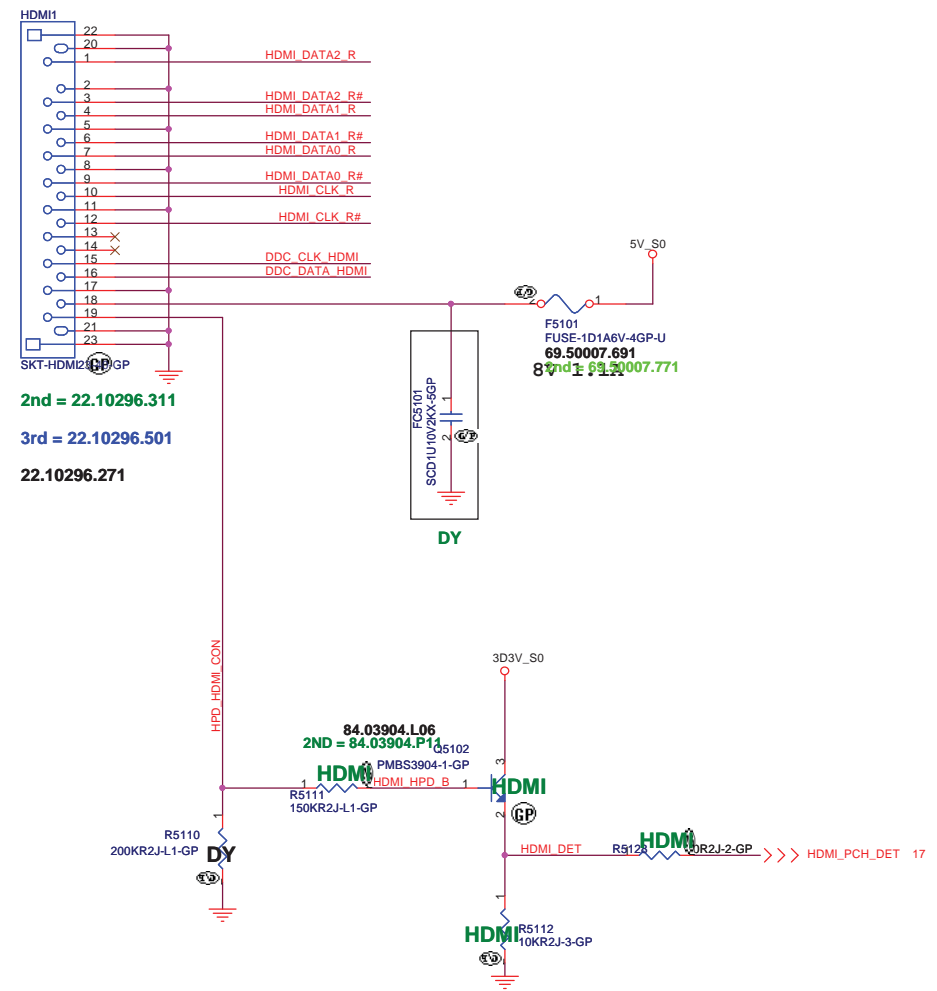
Document Number
Hummingbird1 HR

Rev
-2

Date: Tuesday, April 17, 2012

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HDMI Level Shifter & CONNECTOR



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HR PX

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title		
eDP		
Size	Document Number	Rev
A3	Hummingbird1 HR	-2
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<Variant Name>		
<div>緯創資通Wistron Corporation21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
S-VIDEO		
Size	Document Number	Rev
A4	Hummingbird1 HR	-2
Date:	Tuesday, April 17, 2012	Sheet 53 of 102

(Blanking)

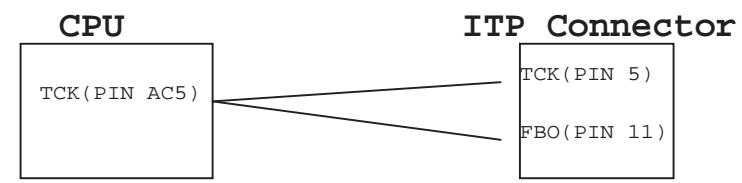
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<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>Hummingbird1 HR</div>	Rev <div>-2</div>
Date <div>Tuesday, April 17, 2012</div>		Sheet <div>54</div> of <div>102</div>

SSID = User.Interface

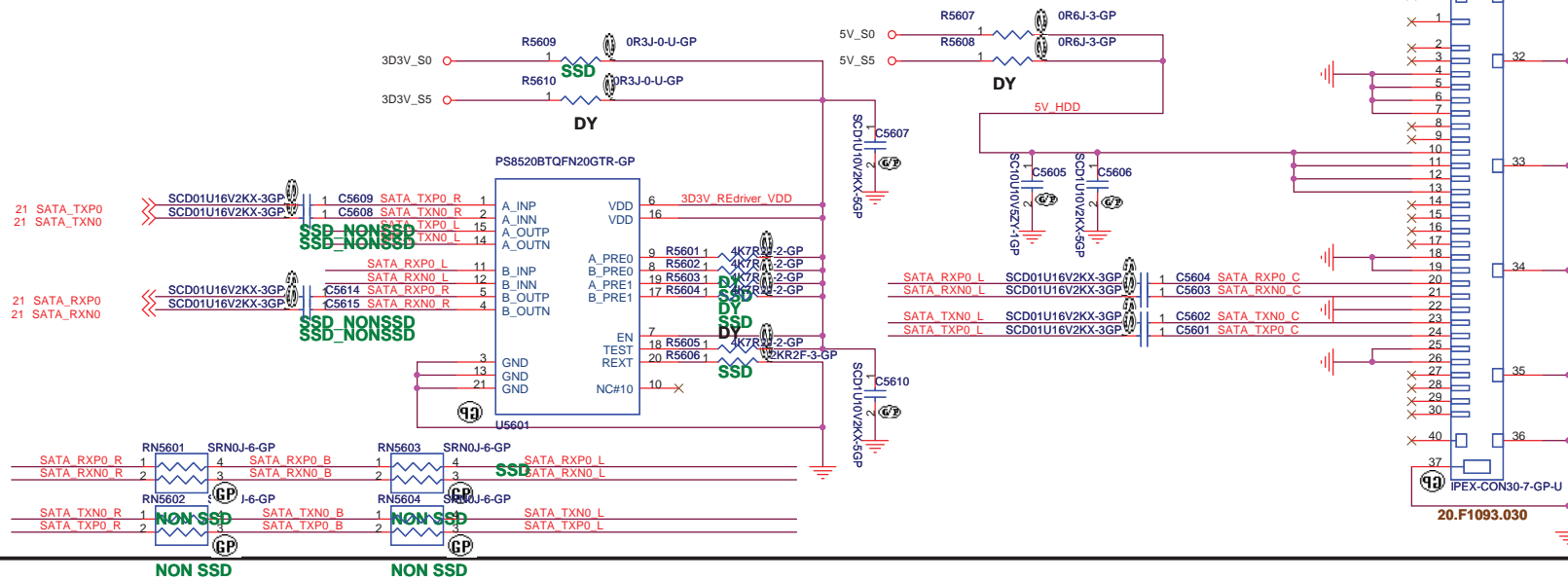
ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



SSID = SATA

SATA HDD Connector



ODD Connector

Without ODD

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<Variant Name>

Title		
HDD/ODD		
Size	Document Number	Rev
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ESATA Power

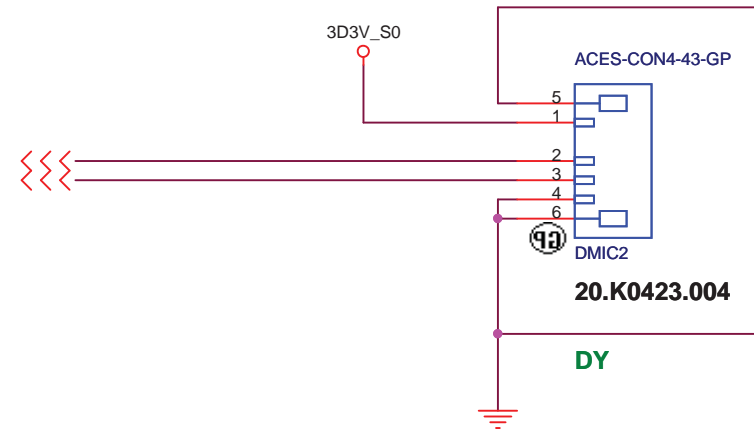
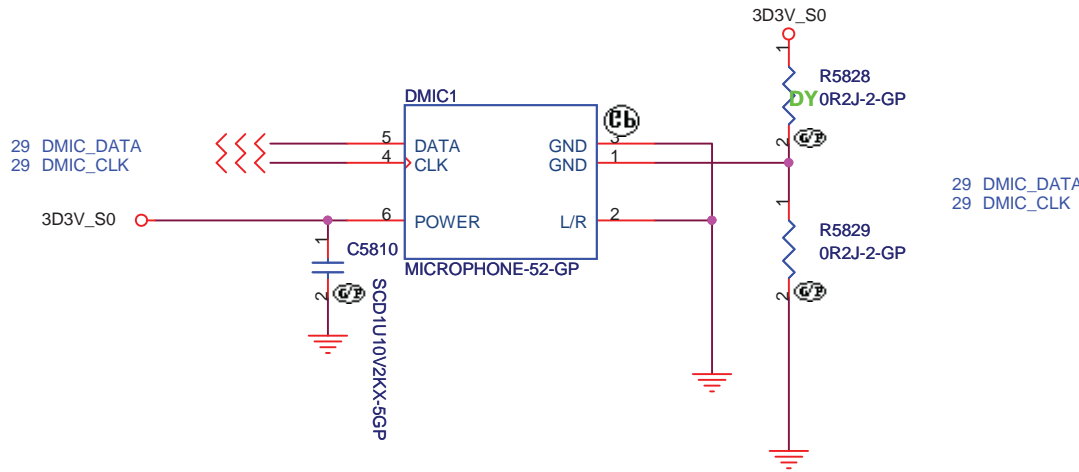
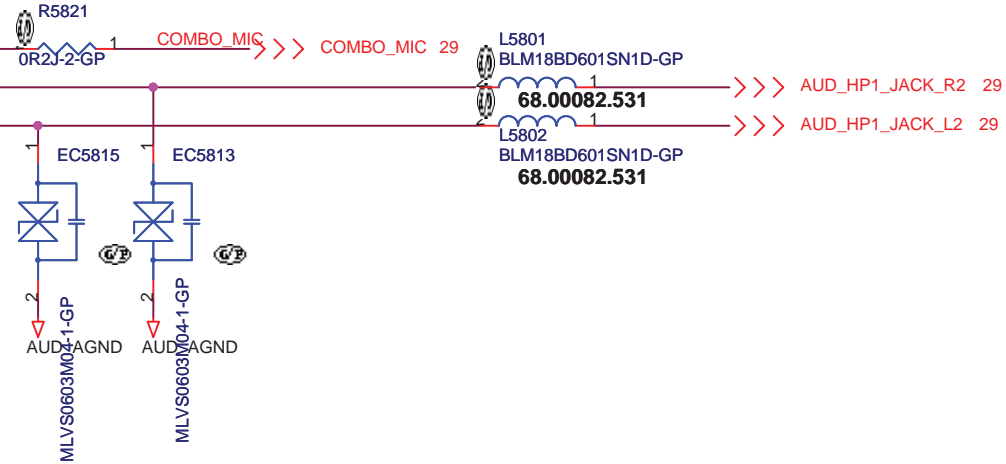
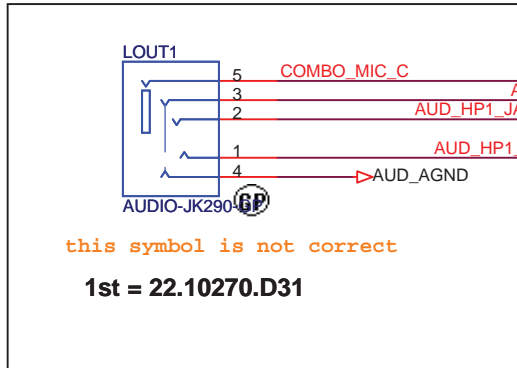
USB CHARGER

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<Variant Name>

<div>緯創資通Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
E-SATA/USB CHARGER		
Size	Document Number	Rev
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SSID = AUDIO



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<Variant Name>

緯創資通 Wistron Corporation
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Title

Audio Jack

Size
A4

Document Number

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Rev
-2

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- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

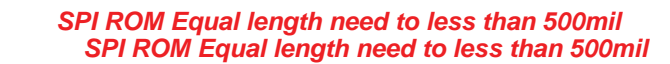
Without LAN

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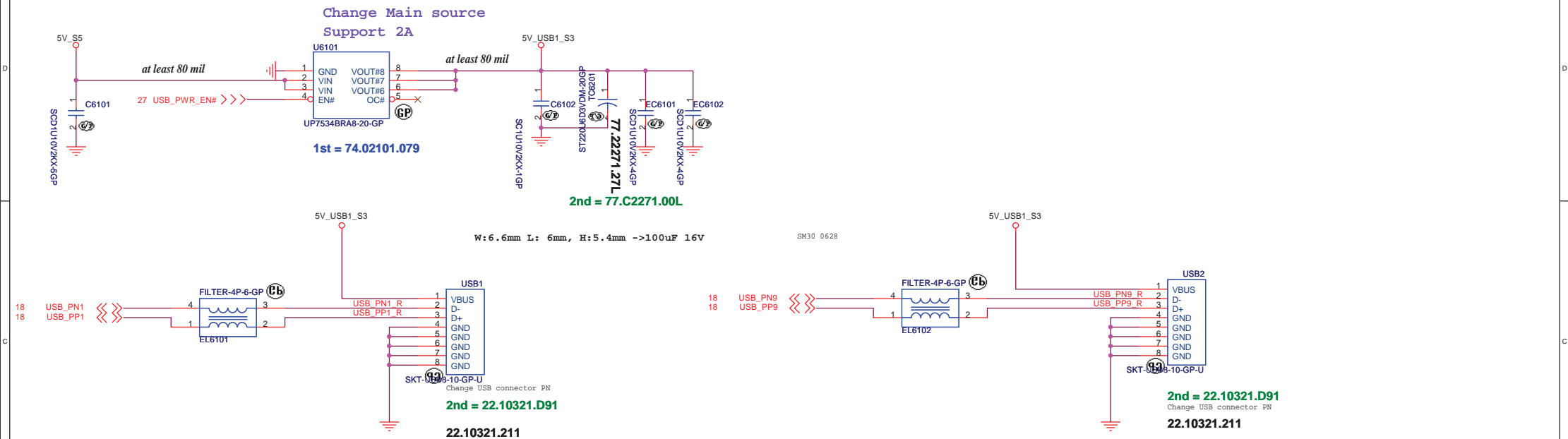
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Title <div>LAN CONNECTOR</div>		
Size <div>A4</div>	Document Number <div>Hummingbird1 HR</div>	Rev <div>-2</div>
Date <div>Tuesday, April 17, 2012</div>		Sheet <div>59</div> of <div>102</div>

```
SSID = Flash.ROM
```



IO Board USB Power



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Blanking

<Variant Name>		
<div>緯創資通Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
USB 3.0 Port		
Size	Document Number	Rev
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SSID = User.Interface
Bluetooth Module conn.

Without BT

<Variant Name>

緯創資通

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Bluetooth

Size
A4

Document Number

Hummingbird1 HR

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-2

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Finger printer

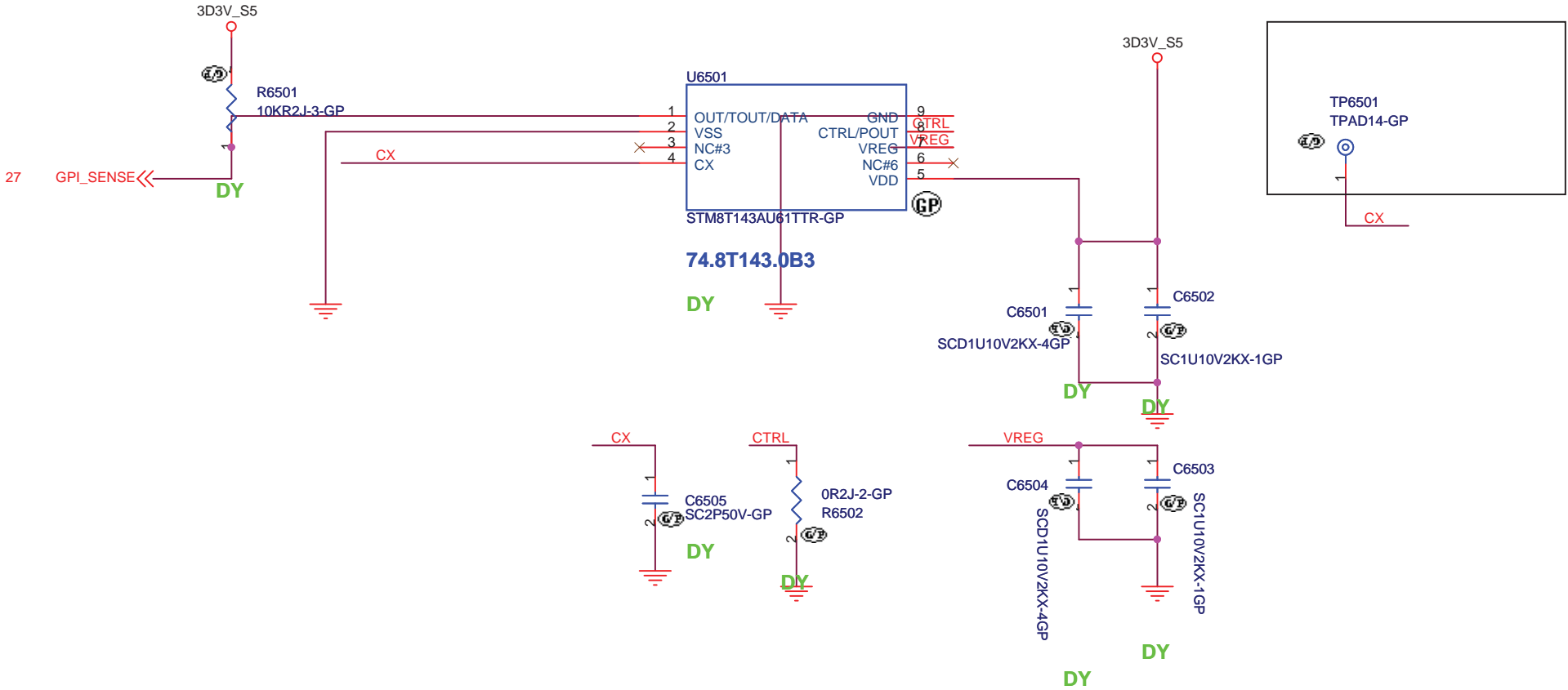
JE40 delete FP function



<Variant Name>		
<div>緯創資通Wistron Corporation21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
RESERVED		
Size	Document Number	Rev
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SSID = Wireless

C Sensor



<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Author	Year	Journal	Volume	Issue	Page
1. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John Doe	1998	Journal of International Economics	50	2	123-145
2. The Impact of the 1997 Asian Financial Crisis on the Japanese Economy	Jane Smith	1998	Journal of International Economics	50	2	146-168
3. The Effect of the 1997 Asian Financial Crisis on the South Korean Economy	Dr. Kim Min-jun	1998	Journal of International Economics	50	2	169-191
4. The Impact of the 1997 Asian Financial Crisis on the Thai Economy	Dr. Sornrat Tang	1998	Journal of International Economics	50	2	192-214
5. The Effect of the 1997 Asian Financial Crisis on the Indonesian Economy	Dr. Bambang Luthfi	1998	Journal of International Economics	50	2	215-237
6. The Impact of the 1997 Asian Financial Crisis on the Philippine Economy	Dr. Cesar P. Reyes	1998	Journal of International Economics	50	2	238-260
7. The Effect of the 1997 Asian Financial Crisis on the Malaysian Economy	Dr. Anwarudin Hassan	1998	Journal of International Economics	50	2	261-283
8. The Impact of the 1997 Asian Financial Crisis on the Singapore Economy	Dr. Lim Joo Ee	1998	Journal of International Economics	50	2	284-306
9. The Effect of the 1997 Asian Financial Crisis on the Hong Kong Economy	Dr. Michael S. Tsang	1998	Journal of International Economics	50	2	307-329
10. The Impact of the 1997 Asian Financial Crisis on the Taiwan Economy	Dr. Sheng-feng Chen	1998	Journal of International Economics	50	2	330-352

MINICARD(WLAN)/ITP CONN

Size
A4

Document Number

Hummingbird1_HR

Rev
2

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SSID = Wireless

Blanking

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<Variant Name>		
<div>緯創資通Wistron Corporation21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
WWAN Connector		
Size	Document Number	Rev
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<Variant Name>

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <div>M-SATA</div>		
Size <div>A4</div>	Document Number <div>Hummingbird1 HR</div>	Rev <div>-2</div>
Date: Tuesday, April 17, 2012		Sheet 67 of 102

SSID = User.Interface

Move to power board

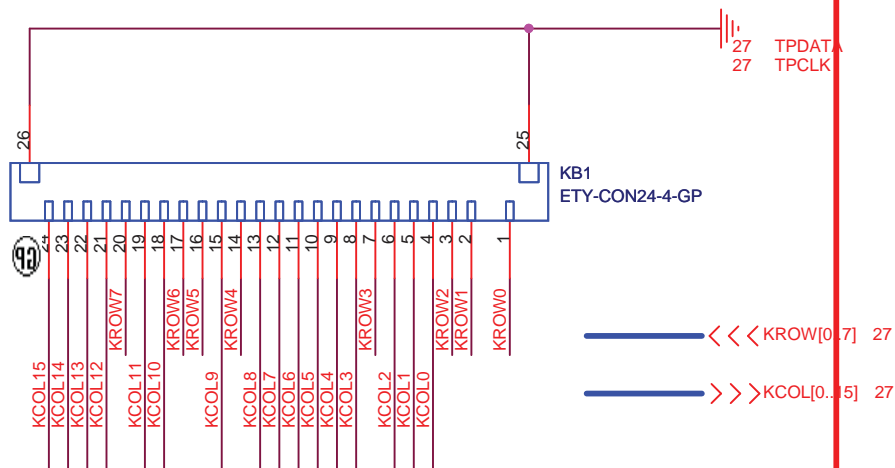
for factory test

<Variant Name>

<div>緯創資通Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
TitleLED Bard/Power Button		
Size Custom	Document NumberHummingbird1 HR	Rev-2
Date: Tuesday, April 17, 2012	Sheet 68	of 102

SSID = KBC

Internal KeyBoard Connector

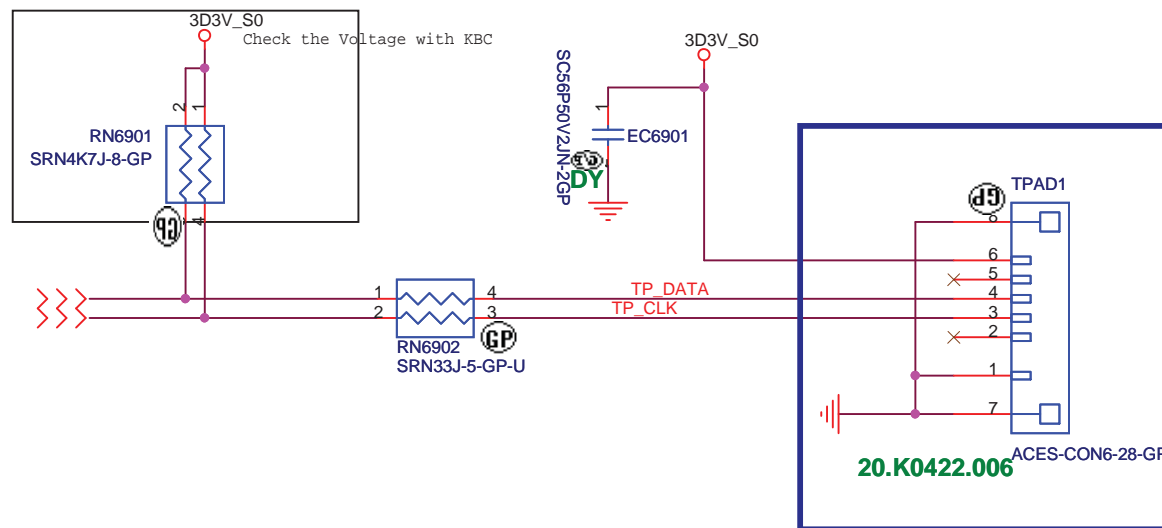


MB 與 KB PIN to PIN

1 K/B 26

Change KB from 下接觸 to 上接觸
KB Pin define need to check again

TOUCH PAD



```
Change back to 1mm pin pitch connector
Switch the pin order      SA
```

D

D

C

C

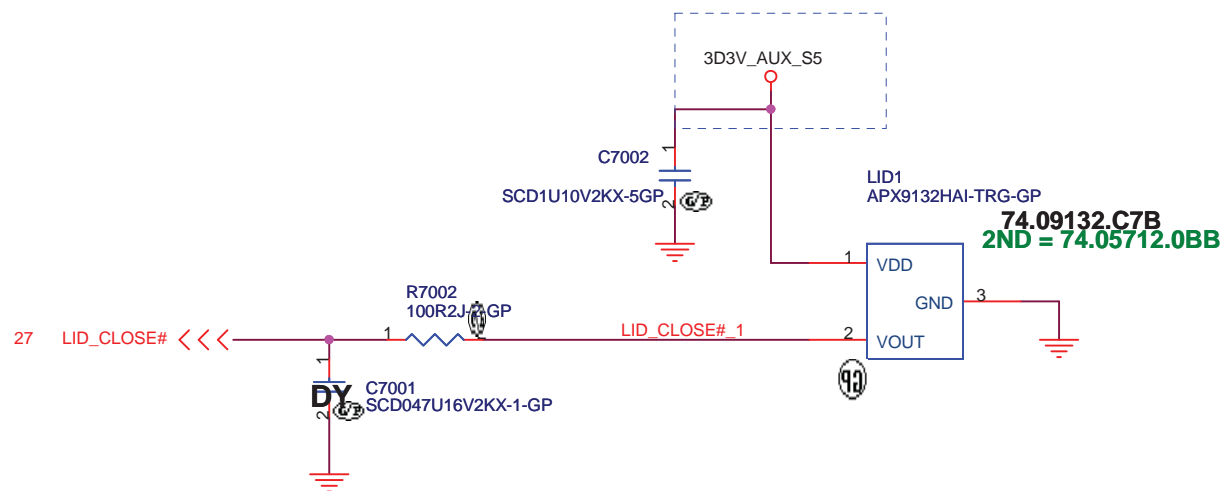
B

B

A

A

Change from 3D3V_AUX_KBC to 3D3V_AUX_S5



<Variant Name>

緯創資通

Wistron Corporation

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Title

Hall Sensor

Size
A4

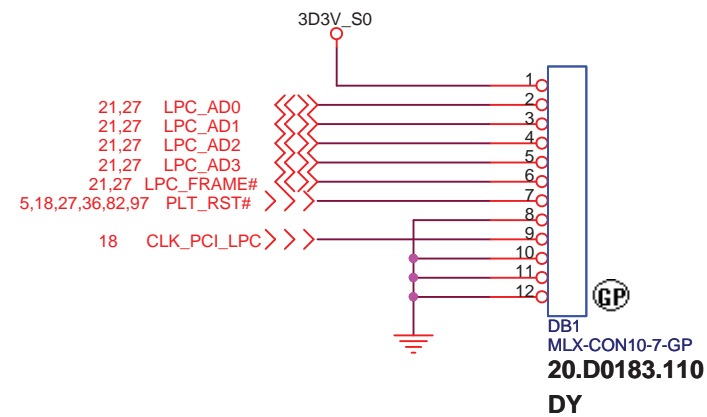
Document Number

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<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

Dubug connector

Size
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<Variant Name>		
<div>緯創資通Wistron Corporation21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
TitleReserved		
SizeA4	Document NumberHummingbird1 HR	Rev-2
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(Blanking)

<Variant Name>

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>Hummingbird1 HR</div>	Rev <div>-2</div>
Date <div>Tuesday, April 17, 2012</div>		Sheet <div>73</div> of <div>102</div>

SD/XD/MS Card Reader

Card reader move to small board

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<Variant Name>

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Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

CARD Reader CONN

Size
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SSID = ExpressCard

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

(Blanking)

<Variant Name>		
<div>緯創資通Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>Hummingbird1 HR</div>	Rev <div>-2</div>
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<Variant Name>		
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TitleReserved		
SizeA4	Document NumberHummingbird1 HR	Rev-2
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(Blanking)

<Variant Name>

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>Hummingbird1 HR</div>	Rev <div>-2</div>
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SSID = User.Interface

Free Fall Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Delete G Sensor Function

Note

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

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<Variant Name>

緯創資通

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Title

Free Fall Sensor

Size
A4

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<Variant Name>		
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TitleReserved		
SizeA4	Document NumberHummingbird1 HR	Rev-2
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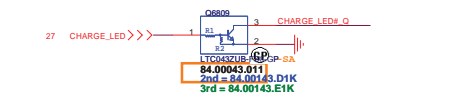
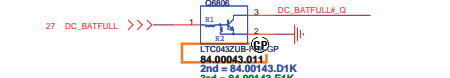
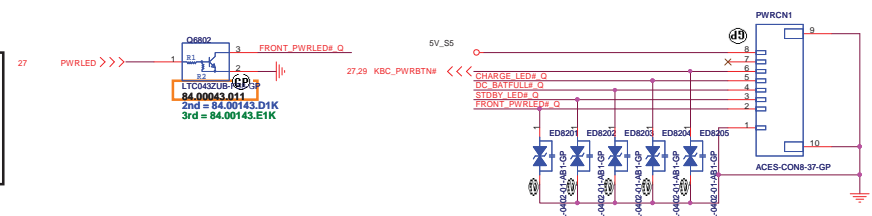
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TitleReserved		
SizeA4	Document NumberHummingbird1 HR	Rev-2
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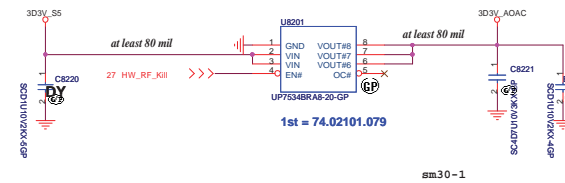
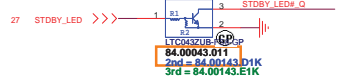
[illegible]

Diagram illustrating the ACES-CON6-40 GP connector. The connector is shown with pins numbered 1 through 40. The diagram includes labels for various components and connections:

- DCBATOUT**: Connected to pin 1.
- PWR1**: Connected to pin 2.
- ACES-CON6-40 GP**: The connector itself.
- 20.F0693.006**: A component connected to pin 3.
- 20.F0818.006**: A component connected to pin 4.
- SK30 0627**: A component connected to pin 5.
- SDU1u6750 x GP**: A component connected to pin 6.
- SDU1u6750 x GP**: A component connected to pin 7.
- SDU1u6750 x GP**: A component connected to pin 8.
- SDU1u6750 x GP**: A component connected to pin 9.
- SDU1u6750 x GP**: A component connected to pin 10.
- SDU1u6750 x GP**: A component connected to pin 11.
- SDU1u6750 x GP**: A component connected to pin 12.
- SDU1u6750 x GP**: A component connected to pin 13.
- SDU1u6750 x GP**: A component connected to pin 14.
- SDU1u6750 x GP**: A component connected to pin 15.
- SDU1u6750 x GP**: A component connected to pin 16.
- SDU1u6750 x GP**: A component connected to pin 17.
- SDU1u6750 x GP**: A component connected to pin 18.
- SDU1u6750 x GP**: A component connected to pin 19.
- SDU1u6750 x GP**: A component connected to pin 20.
- SDU1u6750 x GP**: A component connected to pin 21.
- SDU1u6750 x GP**: A component connected to pin 22.
- SDU1u6750 x GP**: A component connected to pin 23.
- SDU1u6750 x GP**: A component connected to pin 24.
- SDU1u6750 x GP**: A component connected to pin 25.
- SDU1u6750 x GP**: A component connected to pin 26.
- SDU1u6750 x GP**: A component connected to pin 27.
- SDU1u6750 x GP**: A component connected to pin 28.
- SDU1u6750 x GP**: A component connected to pin 29.
- SDU1u6750 x GP**: A component connected to pin 30.
- SDU1u6750 x GP**: A component connected to pin 31.
- SDU1u6750 x GP**: A component connected to pin 32.
- SDU1u6750 x GP**: A component connected to pin 33.
- SDU1u6750 x GP**: A component connected to pin 34.
- SDU1u6750 x GP**: A component connected to pin 35.
- SDU1u6750 x GP**: A component connected to pin 36.
- SDU1u6750 x GP**: A component connected to pin 37.
- SDU1u6750 x GP**: A component connected to pin 38.
- SDU1u6750 x GP**: A component connected to pin 39.
- SDU1u6750 x GP**: A component connected to pin 40.



Q6803



SPK1

5

1

2

3

4

6

GP

ACES-COM4-17-GP-U1

2nd = 20.F1686.004

20.F1621.004

ECR202

ECR201

ECR203

ECR204

69.80024.078

69.80024.011

69.80024.011

69.80024.011

M.U. G040223N05GP-U1

M.U. G040223N05GP-U1

M.U. G040223N05GP-U1

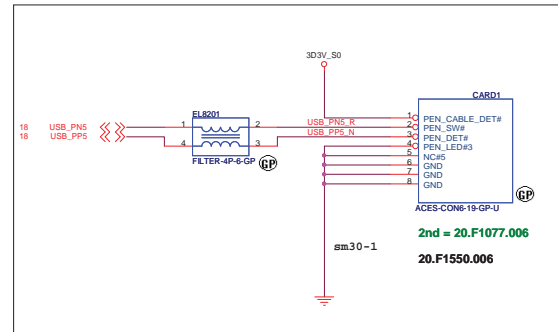
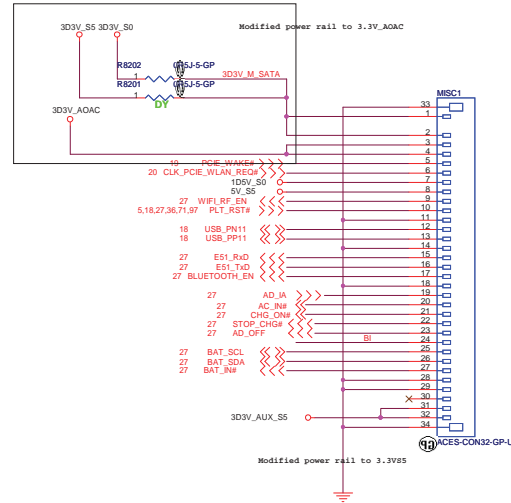
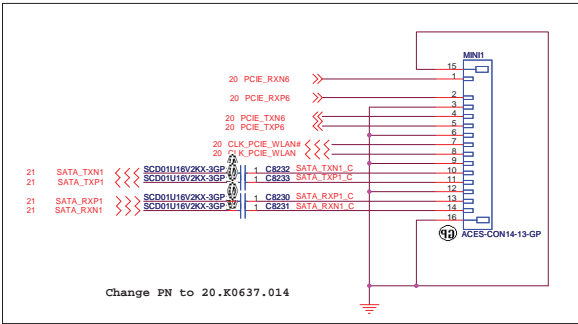
M.U. G040223N05GP-U1

AUD_SPK_L+ 29

AUD_SPK_L- 29

AUD_SPK_R+ 29

AUD_SPK_R- 29



SPK1

5

1

2

3

4

6

GP

ACES-COM4-17-GP-U1

2nd = 20.F1686.004

20.F1621.004

ECR202

ECR201

ECR203

ECR204

69.80024.0789.80024.011

69.80024.011

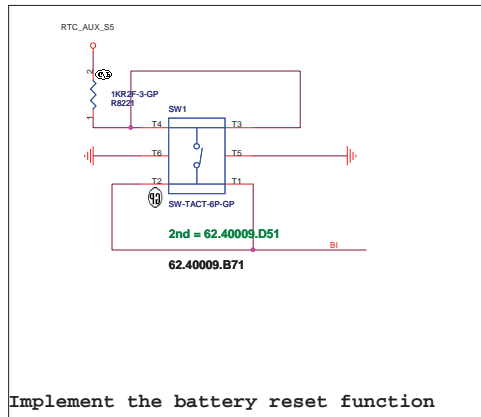
69.80024.011

AUD_SPK_L+

AUD_SPK_L-

AUD_SPK_R+

AUD_SPK_R-



SPK1

5

1

2

3

4

6

GP

ACES-COM4-17-GP-U1

2nd = 20.F1686.004

20.F1621.004

ECR202

ECR201

ECR203

ECR204

69.80024.0789.80024.011

69.80024.011

69.80024.011

AUD_SPK_L+

AUD_SPK_L-

AUD_SPK_R+

AUD_SPK_R-

SPK1

5

1

2

3

4

6

GP

ACES-COM4-17-GP-U1

2nd = 20.F1686.004

20.F1621.004

EC8202

EC8201

EC8203

EC8204

69.80024.011

69.80024.011

69.80024.011

69.80024.011

MU.G040220N05BP-G1

MU.G040220N05BP-G1

MU.G040220N05BP-G1

MU.G040220N05BP-G1

<<< AUD_SPK_L- 29

<<< AUD_SPK_L+ 29

<<< AUD_SPK_R- 29

<<< AUD_SPK_R+ 29

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

GPU Memory(2/5)

Hummingbird1 HR

Title

Size

Custom

Date: Tuesday, April 17, 2012

Document Number

Rev

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<Variant Name>		
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Title		
GPU DPPWR/GND(5/5)		
Size	Document Number	Rev
A3	Hummingbird1_HR	-2
Date:	Tuesday, April 17, 2012	Sheet 87 of 102

<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipai Hsien 221, Taiwan, R.O.C.

Title

GPU-VRAM1,2 (1/4)

Size

Document Number

Rev

Custom

Hummingbird1 HR

-2

Date: Tuesday, April 17, 2012

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<Core Design>

<div>緯創資通Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
TitleGPU-VRAM3,4 (2/4)		
Size Custom	Document NumberHummingbird1 HR	Rev-2
Date:Tuesday, April 17, 2012	Sheet89	of102

<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU-VRAM5,6 (3/4)

Size
Custom

Document Number

Rev

Hummingbird1_HR-2

Date: Tuesday, April 17, 2012

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<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU-VRAM7,8 (4/4)

Size

Document Number

Rev

Custom

Hummingbird1 HR

-2

Date: Tuesday, April 17, 2012

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TitleDISCRETE VGA POWER		
SizeA4	Document NumberHummingbird1 HR	Rev-2
DateTuesday, April 17, 2012	Sheet93	of102

LVDS Channel A

Blanking

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<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

LVDS Switch

Size
A4

Document Number

Hummingbird1 HR

Rev
-2

Date: Tuesday, April 17, 2012

Sheet 94 of 102

Blanking

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<Variant Name>		
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Title <div>CRT Switch</div>		
Size <div>A4</div>	Document Number <div>Hummingbird1 HR</div>	Rev <div>-2</div>
Date: Tuesday, April 17, 2012		Sheet 95 of 102

SSID = SDIO

Blanking

<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

TOUCH PANEL

Size
A4

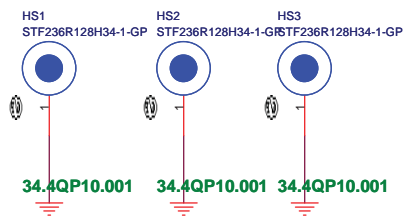
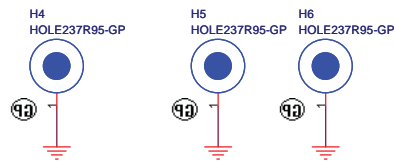
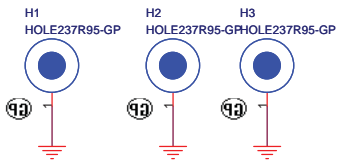
Document Number

Hummingbird1 HR

Rev
-2

Date: Tuesday, April 17, 2012

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Check test point



Test Point放在Dimm Door打開可量測處



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title UNUSED PARTS/EMI Capacitors		
Size A3	Document Number Hummingbird1 HR	Rev -2
Date Tuesday, April 17, 2012	Sheet 97	of 102

- (1) change U6001 to socket 62.10089.001
- (2) change SW_L1 and SW_R1 PN to 『62.40089.221』
- (3) KI.G6501.001 / IC BD82HM65 SLH9D MM#908753 B2 FCBGA 989
KI.G6501.004 / IC BD82HM65 SLJ4P MM#914377 B3 FCBGA989P
- (4)U3101 change PN to 71.08158.M02
- (5)DM2 1st -> change PN to 62.10024.G01
- (6) IMIC1 =>82.40012.001
- (7) RJ1 =>22.10177.J71
- (8) CPU1 =>1st change PN to 62.10055.321
- (9) USB2 =>1st change PN to22.10218.G01 -> only Lab stage

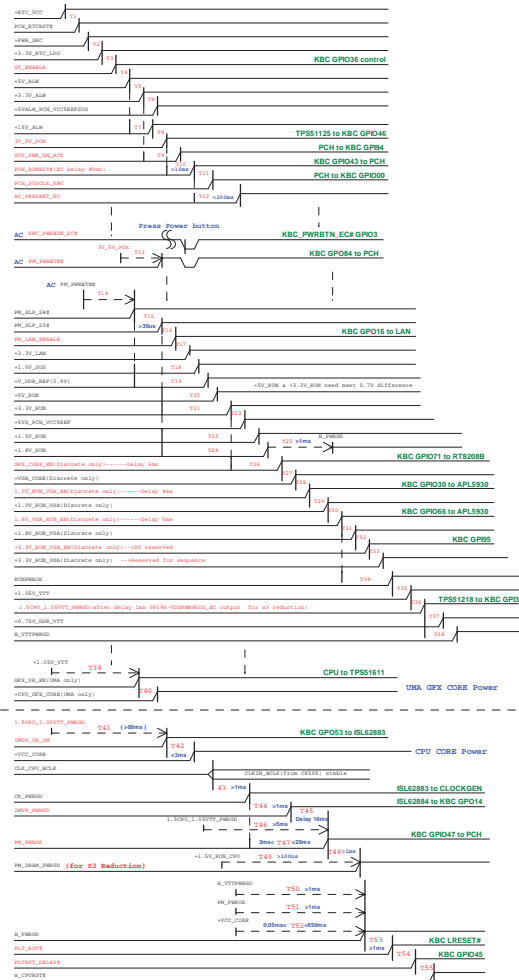
	-SA
	-SB
	-1
	-2

[Lab] S01G ==>1st
S02G ==>2nd(NEC Cap)

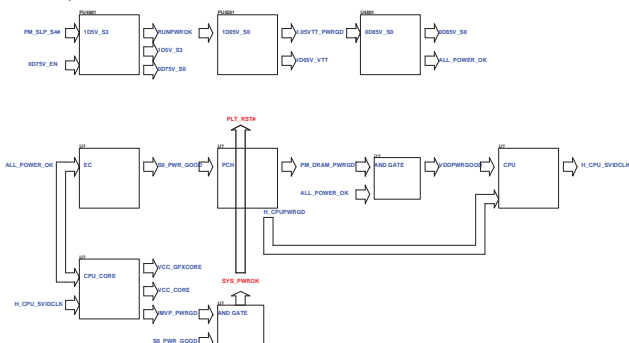
Coin Battery:
1st:23.20068.001
2nd:23.22063.001

(AC mode)

red word: XBC GPIO

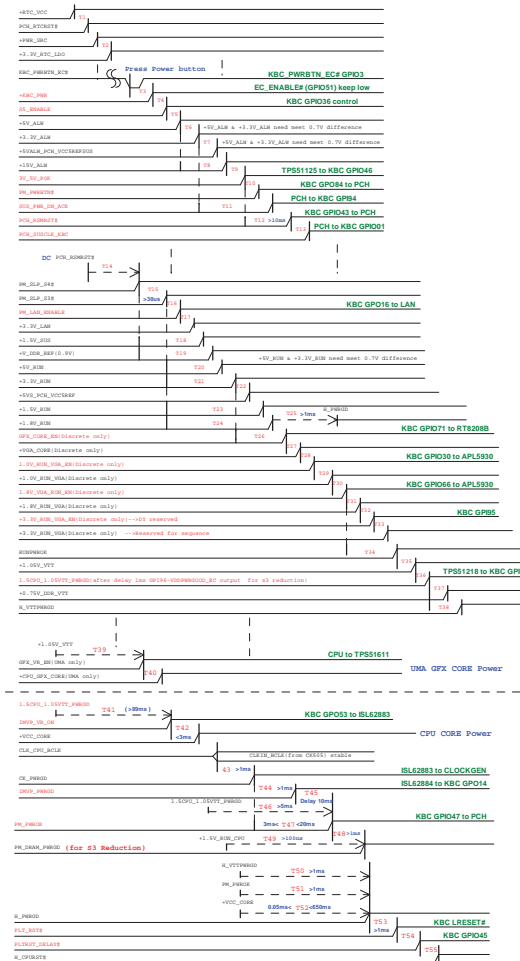


Power Sequence

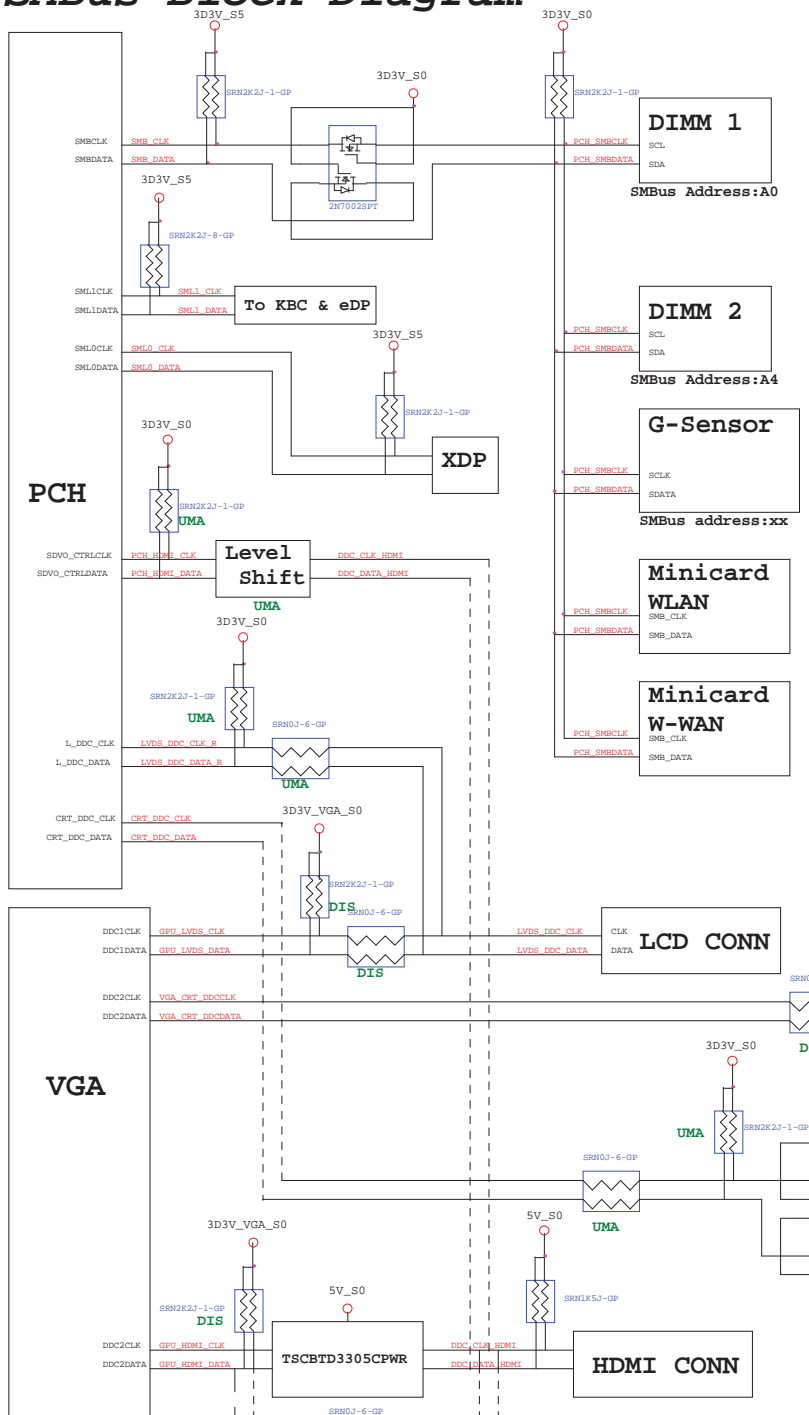


(DC mode)

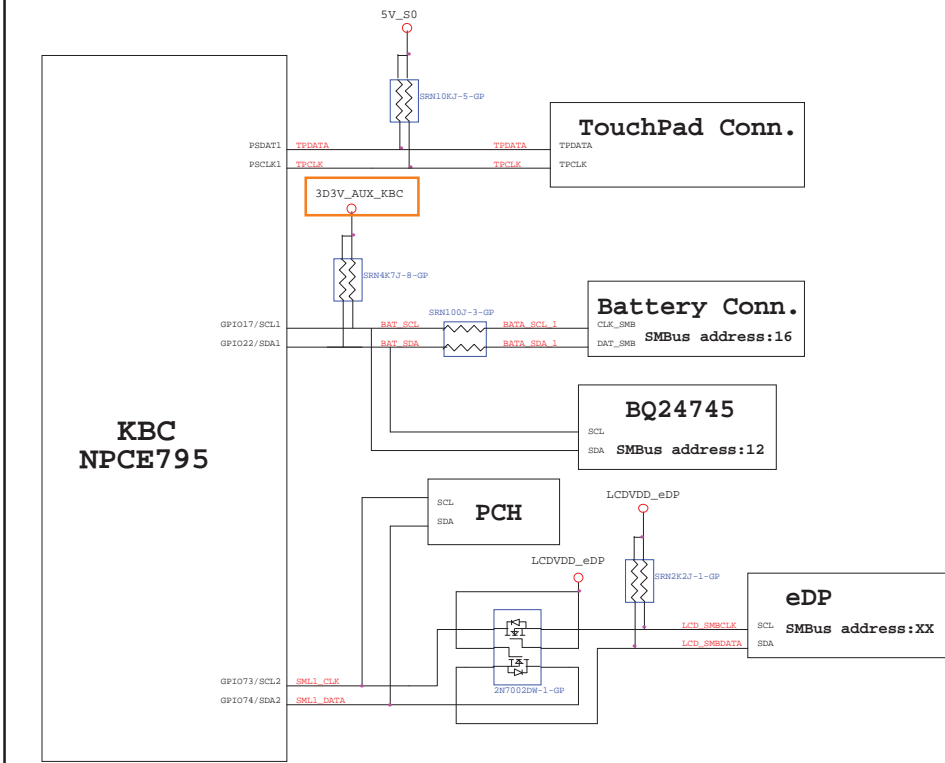
red word: XBC GPIO



PCH SMBus Block Diagram

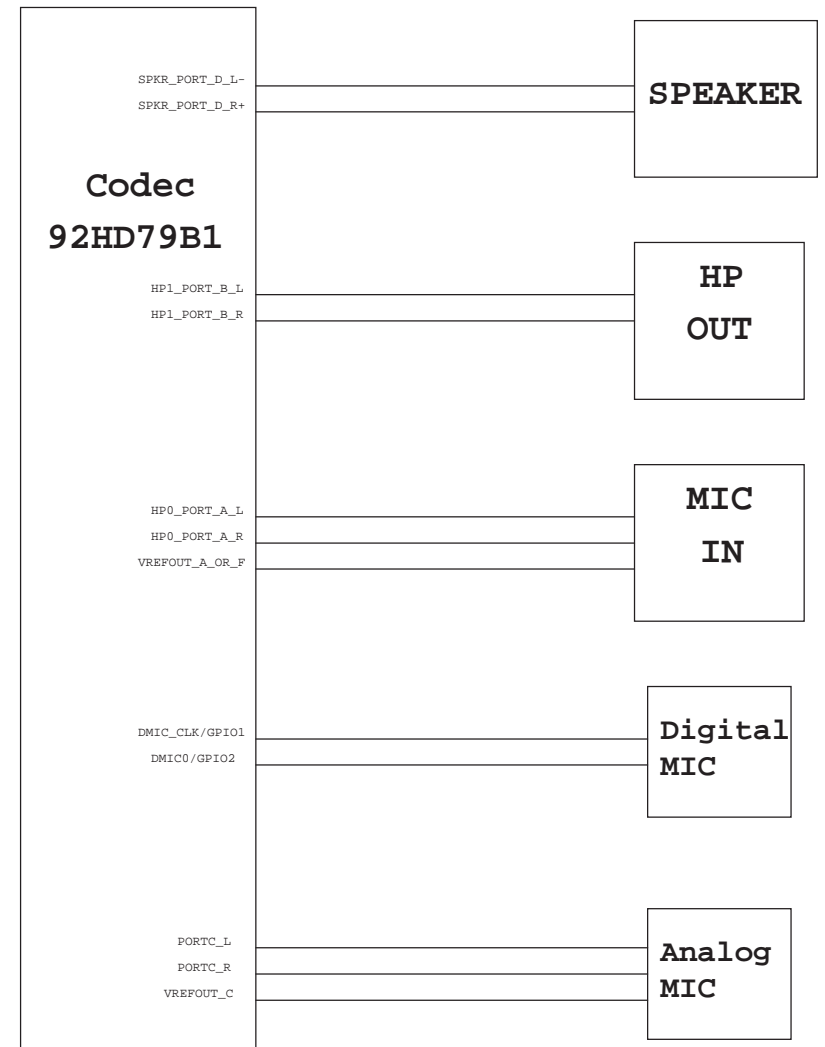


KBC SMBus Block Diagram



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Audio Block Diagram



<Variant Name>			
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Title			
Thermal/Audio Block Diagram			
Size	Document Number		Rev
Custom	Hummingbird1_HR		-2
Date:	Tuesday, April 17, 2012	Sheet 102 of 102	